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Analysis and design of grid-connected 3-phase 3-level AT-NPC inverter for low-voltage applications

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Abstract: The 3-level T-type neutral point clamped (T-NPC) inverter has become the most popular multilevel inverter used in low-voltage applications. However, the realization of a bidirectional switch located at the midpoint leg of the T-NPC inverter is achieved using two insulated gate bipolar transistors (IGBTs) with two antiparallel diodes. Power dissipation in these switches is high since there are two semiconductors (an IGBT and a diode) in the current path at the midpoint leg. Switch losses can be reduced and thus the highest conversion efficiency can be achieved if the bidirectional switches in the T-NPC inverter are replaced by highly efficient reverse-blocking IGBTs (RB-IGBTs). The objective of this paper is to assess the performance of a 3-phase 3-level grid-connected advanced T-NPC (AT-NPC) inverter with RB-IGBT for low-voltage applications. This paper describes the operating principle of the grid-connected AT-NPC inverter, analyzes the power losses, and discusses the control strategy. A 1.7-kW laboratory prototype is designed and built to verify the feasibility and the effectiveness of the proposed 3-phase 3-level grid-connected AT-NPC inverter. Real-time control of the inverter is experimentally achieved using a dSPACE DS1103 controller. The experimental results show that the efficiency of the proposed grid-connected inverter is about 96.3%.

Key words: RB-IGBT, advanced T-NPC, grid-connected, highly efficient inverter, three-level inverter, low voltage

1. Introduction

In many power electronics applications, conversion of power from DC to AC is a significant subject. To achieve this goal, inverters are used in many industrial applications such as renewable energy systems, induction heating, electric vehicles, and uninterruptible power supplies. In the literature, inverters are categorized based on input source type, grid interaction, control technique, output voltage level, etc. However, efficiency and reliability are the main considerations for designing and investigating the procedures of an inverter [1,2].

Multilevel inverters (MLIs) can generate an output waveform very similar to a sinusoidal wave, with lower harmonic distortion compared to 2-level inverters [3]. Because of these features, MLIs are highly preferred for their high efficiency and high power quality applications. Therefore, much research is still ongoing for increasing the efficiency of MLIs [4,5]. Basically, MLIs can be found in neutral point-clamped (NPC) flying capacitor, and cascade H-bridge topologies [6,7]. Many modifications and combinations of these topologies have been investigated to meet high efficiency requirements. Among these, T-type NPC (T-NPC) inverters are among the most preferred topologies [8,9]. Up to medium switching operation frequency ($<$24 kHz), T-NPC inverters are more efficient than other MLIs [10]. In addition, T-NPC inverters have low total harmonic distortion (THD)

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(an advantage of classical NPC inverters) and simple operation principles (an advantage of 2-level inverters) [8]. Furthermore, the modulation strategy used in 3-level NPC inverters can also be applied to a T-NPC inverter [11].

In addition to topological differences, the internal structure of used semiconductor switches, modulation, and switching techniques are important factors regarding the efficiency of inverters. In industrial applications, the conventional insulated gate bipolar transistor (IGBT) structure is still one of the most preferred switching devices [12]. However, the reverse blocking voltage capability of the conventional IGBT is very low. For this reason, conventional IGBTs are used with freewheeling diodes (FWDs) in various applications. To provide both reverse and forward voltage-blocking capabilities, a reverse blocking IGBT (RB-IGBT) is designed [13,14]. Moreover, in some applications, such as the T-NPC inverter, a bidirectional switch is formed by using two conventional IGBTs with two antiparallel FWDs. On the other hand, a bidirectional switch can be created with only two RB-IGBTs, which do not require FWDs [12,15]. The structures of the bidirectional switch created with conventional IGBT and RB-IGBT are shown in Figure 1. By using the RB-IGBT instead of a conventional IGBT in the DC-link midpoint of the T-NPC inverter, an advanced T-NPC (AT-NPC) inverter structure is obtained. This structure is more efficient than the T-NPC inverter because switching and conduction loses are reduced [12,15].

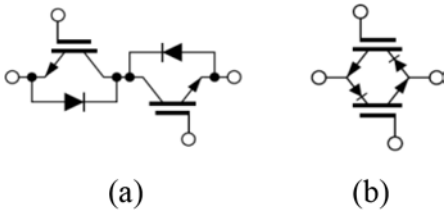


Figure 1. Bidirectional switch with (a) conventional IGBTs, (b) RB-IGBTs.

This paper analyzes 3-level NPC topologies for low-voltage application regarding various features, especially efficiency. After topological advantages and disadvantages are discussed, the proposed AT-NPC type inverter is introduced. Additionally, its operational principles and switching states are detailed. In order to analyze the efficiency of the AT-NPC inverter, switching and conduction loss calculation methods are addressed. Control of the 3-phase 3-level grid-connected AT-NPC inverter is achieved digitally using dSPACE hardware. The experimental results show that the designed system meets the high efficiency demand for low-voltage grid-connected inverter applications.

2. Topologies

2.1. Topological structures

Recently, 2-level inverters were replaced by MLIs due to the low level THD output of the latter. In particular, 3-level and highly efficient inverters are favored for low-voltage applications [11,16]. Low-level THD causes a decrease in filter requirement, which reduces the size of the inverter and increases overall efficiency. One of the most popular topologies in terms of high-voltage applications is the NPC. T-NPC inverters (a derivative of the classical NPC topology) are also widely preferred in low-voltage applications. The structures of classical NPC and T-NPC inverters are shown in Figures 2a and 2b, respectively. In Figure 2b, the T-NPC topology is created with common emitter connection configurations of T3 and T4. Since the common collector configuration requires an extra gate drive, the employment of a common emitter configuration is more reasonable. T-NPC and 2-level

inverters have several common advantages, including low conduction losses and the use of a simple switching technique. T-NPC inverters also have common advantages with 3-level inverters, including low switching losses and high quality output voltage [8,16,17].

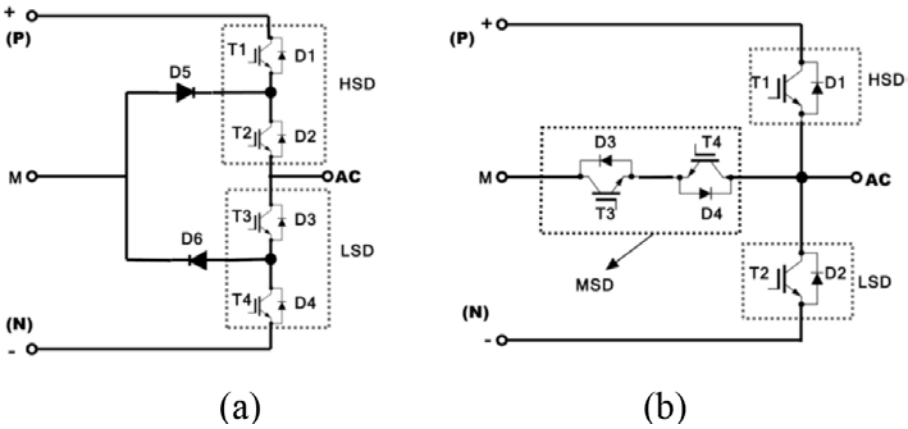


Figure 2. Structure of (a) classical type NPC, (b) T-type NPC.

In low-voltage applications, e.g., 650-V DC-link voltage, the high-side device (HSD), T1/D1, and low-side device (LSD), T2/D2, need to block the full DC-link voltage in the T-NPC topology. On the other hand, midpoint side devices (MSDs), namely T3/D3 and T4/D4, do not need to block the full DC-link voltage. In this case, MSDs must block just half of the DC-link voltage. This means that in the T-NPC topology, MSDs with a low-voltage rating can be employed. As a result, MSDs provide low switching and conduction losses despite two series-connected switches. In medium- or high-voltage applications, whenever the AC side is connected to positive (P) or negative (N) terminals, the number of series-connected switching devices is important, as the blocked voltage is shared between the devices. However, in low-voltage applications, the blocked voltage is not too high for modern semiconductor switching devices. In the case of NPC inverter operation, the conduction path includes two switching devices. In contrast, in the case of T-NPC inverter operation, conduction paths include only one switching device, the HSD or the LSD. Therefore, conduction losses can be reduced significantly using T-NPC topology instead of NPC topology. Thus, T-NPC topology is more advantageous than NPC topology.

In T-NPC topology, each MSD consists of an IGBT with an antiparallel diode, in which the midpoint leg contains two IGBTs with two antiparallel diodes. When the midpoint of the T-NPC inverter clamps to the AC side, two series of semiconductor forward voltage drop (T3, D4 or T4, D3) occur. This disadvantage of the T-NPC topology can be removed using an AT-NPC topology, wherein the RB-IGBT is employed at the midpoint leg of the inverter. A one-phase equivalent circuit diagram of the AT-NPC is shown in Figure 3. The conduction loss of the AT-NPC inverter is lower than that of the T-NPC inverter due to the employment of the RB-IGBT at the midpoint leg. Moreover, the leakage current of the RB-IGBT is lower than that of the classical IGBT [18].

2.2. Switching configuration and commutation

In applications, inverter control is achieved with various control techniques having certain limitations. Switching signals are produced from the employed control techniques, and these signals form the switching configuration. Moreover, precautions against detrimental situations, such as short circuits, can be taken while switching signals are generated. For these reasons, it is important to examine the switching state of an inverter.

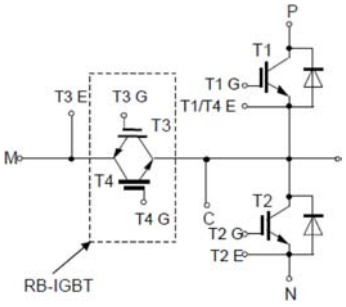


Figure 3. One-phase equivalent circuit of AT-NPC inverter.

In the AT-NPC inverter, 4 switches are employed and consequently 16 different switching state combinations emerge. All possible switching states of the AT-NPC are given in Table 1. The first 8 states are appropriate for inverter operation and do not include any destructive states. However, the other states cause undesirable situations such as full or half DC-link short circuit. After all switching states are considered, commutation and current paths should be investigated. The output of the AT-NPC inverter is connected to P, N, and M, corresponding to $+V_{DC}/2$, $-V_{DC}/2$, and voltage outputs, respectively. These output voltage levels can be easily achieved. For instance, only T1 can be closed for a positive voltage level; similarly, only T2 can be closed for a negative voltage level. However, current direction is not considered with this method. A modulation strategy, such as pulse width modulation (PWM), is used to obtain the mentioned output voltage levels that are independent from the current direction. Table 2 shows the AT-NPC inverter output voltage level with the switching configuration. This configuration is obtained with a sinusoidal PWM modulation strategy and works independently of the current direction. For example, if T1 and T4 are switched (SW) and T3 is turned to the ON state, then the inverter output (V_{out}) shows $+V_{DC}/2$ voltage level, which is independent of the current direction. To investigate the current independency in detail, an inductive load situation can be considered, as seen in Figure 4. In this figure, since the voltage and current are not in phase, there are 4 different operating areas. In operating area 1, voltage and current are positive. If we switch T1 and T4 opposed, positive and midpoint voltage levels (0) are observed at the output of the inverter. However, in the positive voltage area, the current direction can be changed to negative, as seen in operating area 4. In this case, T3 is always kept in the ON state to provide the current path. Figures 5a and 5b show positive and negative current paths in positive voltage, respectively. For the positive direction, the current flows over the T1 and T4 switches, whereas the current flows over the D1 and T3 switches for the negative direction. In operating area 3, voltage and current directions are negative. As seen in Figure 5c, T2 and T3 are switched oppositely to obtain negative voltage. However, the current direction can be changed to positive, as in the case of operating area 2. To provide a positive current path in negative voltage, T4 is always kept in the ON state. Figures 5c and 5d show positive and negative current paths in negative voltage, respectively. For the negative direction, the current flows over the T2 and T3 switches, whereas the current flows over the D2 and T4 switches for the positive direction.

2.3. Power loss calculation

In inverter applications, DC power is converted to AC by means of a semiconductor power switch. When using a power semiconductor, minimizing the switch's loss is the main consideration. When an IGBT is employed as the power switch, some power losses occur because of the IGBT's nonideal internal structure. Figure 6 gives the switching waveform of an IGBT. This figure can be evaluated in three different parts regarding power loss calculation. Two of the three parts are categorized as switching losses and the other is the conduction loss.

Table 1. Switching states of AT-NPC.

	Switching states															
Switch	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}	S_{15}	S_{16}
T1	0	1	0	0	0	0	0	1	1	0	1	1	1	1	1	0
T2	0	0	1	0	0	0	1	0	1	1	0	1	1	1	0	1
T3	0	0	0	1	0	1	0	1	1	1	1	0	1	0	0	1
T4	0	0	0	0	1	1	1	0	1	1	1	1	0	0	1	0

Table 2. Inverter output voltage with switching states.

V_{out}	T1	T2	T3	T4
$+V_{DC}/2$	SW	OFF	ON	SW
0	SW	OFF	ON	SW
	OFF	SW	SW	ON
$-V_{DC}/2$	OFF	SW	SW	ON

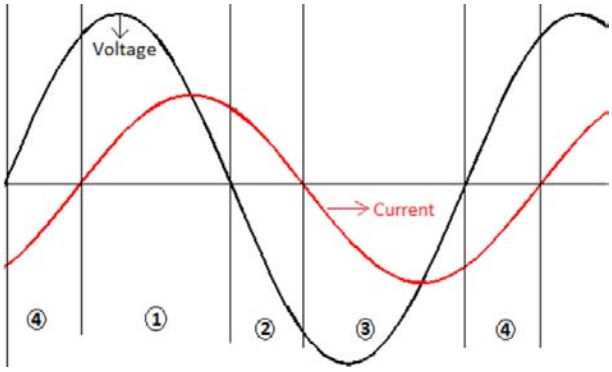


Figure 4. Output voltage and current of an inverter with inductive load.

Switching losses comprise turn-on and turn-off losses. Turn-on and turn-off behaviors of IGBTs were discussed in detail in [19] and [20], respectively. After completing the turn-on transient, the IGBT turns to the ON state and conducts the collector current (I_C), where the overlapping of collector-emitter on-state voltage (V_{CE-on}) and collector current causes conduction loss. The factors affecting conduction loss were given in [13]. According to [21], IGBT turn-on losses are calculated with:

$$W_{\text{turn-on}} = V_{CE}[\frac{(I_L + I_{RR})(t_r + t_a)}{2} + \frac{I_L t_b}{2} + \frac{I_{RR} t_b}{3}], \tag{1}$$

where I_{RR} is reverse recovery current, t_r is current rising time, and t_a and t_b are reverse recovery times. A typical IGBT's turn-off losses depend on delay time (t_d), fall time (t_f), and tail time (t_{tail}) parameters and are calculated as follows:

$$W_{\text{turn-off}} = V_{CE}[\frac{11 I_L t_f}{20} + \frac{I_L t_d}{2} + \frac{I_L t_{tail}}{20}]. \tag{2}$$

The conduction loss is given by:

$$W_{\text{on-state}} = I_L[dT_{sw} - t_a + t_b + t_r)], \tag{3}$$

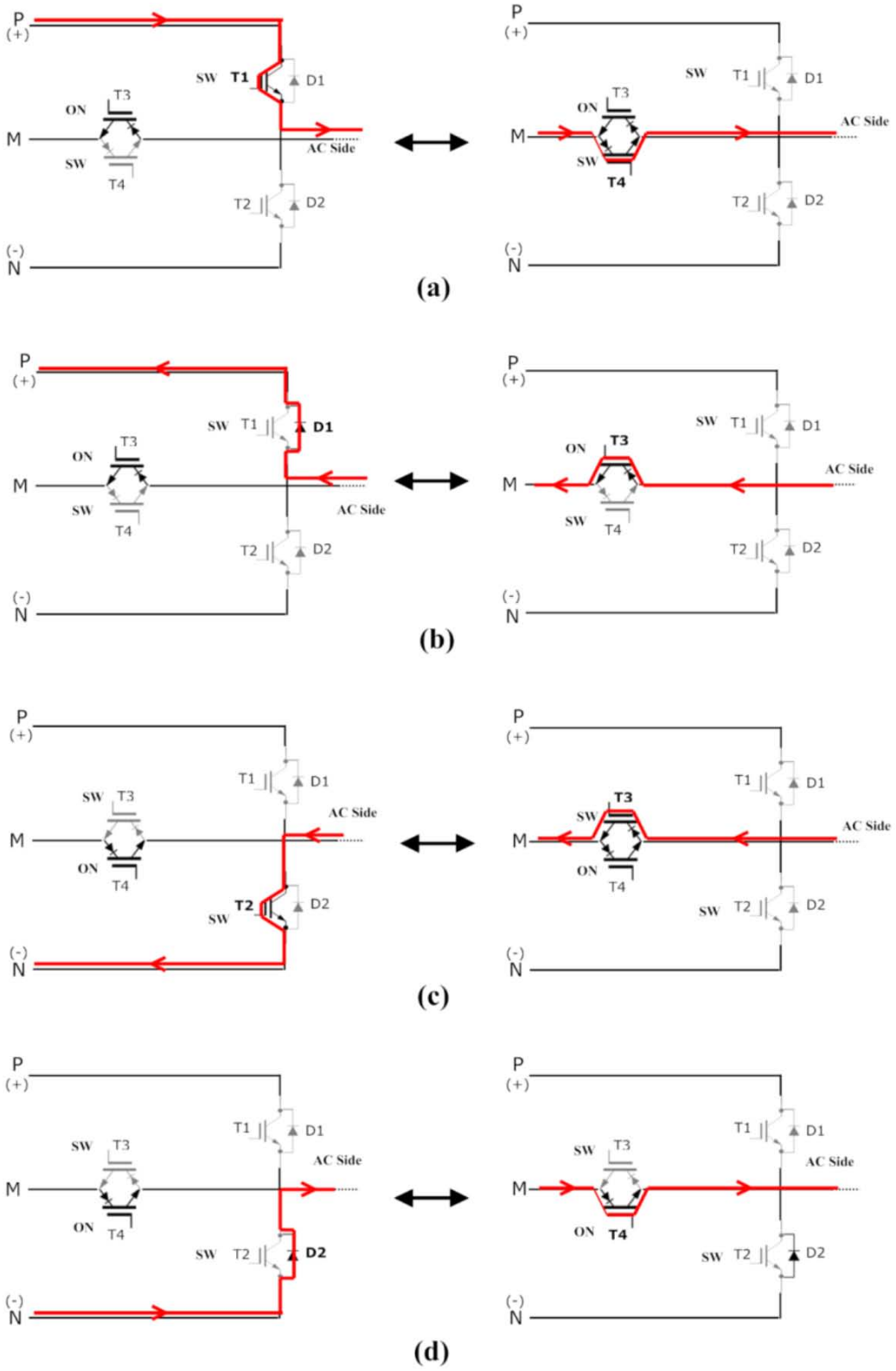


Figure 5. Commutation path for (a) positive voltage and positive current, (b) positive voltage and negative current, (c) negative voltage and positive current, (d) negative voltage and negative current.

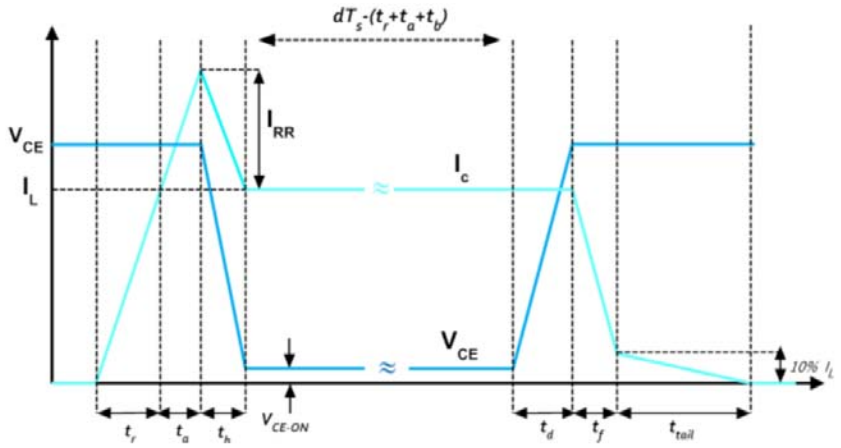


Figure 6. Switching waveform of an IGBT for power loss calculation.

where T_{sw} is the switching period and $d$is the duty cycle. Total power loss of the IGBT is calculated by an integral of switching and conduction loss over the grid period as:

$$P_{loss} = \frac{1}{T_g} \sum_{i=1}^{N} [W_{turn-on}(i) + W_{turn-off}(i) + W_{on-state}(i)], \tag{4}$$

where i symbolizes one switching cycle, T_g is the grid period, and $N$is the total switching cycle in the grid period.

3. Experimental system design

In Figure 7, the system configuration of the designed 3-phase 3-level grid-connected AT-NPC with RB-IGBT is depicted. As seen in the figure, on the DC side, a programmable voltage source is used as a renewable energy source and two DC-link capacitors are connected in series to obtain the neutral point requirement. In the output of the current controlled inverter, an LC-type filter is used to reduce generated current harmonics. The current, whose harmonics level is minimized, splits into two directions at the point of common coupling (PCC), wherein the 3-phase local load unit and 3-phase grid are connected. Three current and voltage sensors are used at the output of the filter and at the grid side, respectively. The acquired current and voltage information is evaluated in dSPACE, which is used as a controller to provide grid synchronization and tracking of the reference current value. After evaluation of the voltage and the current information by the control techniques, PWM signals are generated with dSPACE. Before PWM signals are applied to IGBTs, the IGBT driver board and isolation/protection board are used to increase the dSPACE digital output signals to an appropriate level.

The control technique used in this work has two main objectives. One is to synchronize the generated current with the grid voltage, and the other is to track the reference current value of the generated current. In Figure 8, the control block diagram of the designed system is given. As can be seen in the figure, the phase-locked loop (PLL) algorithm and $d-q$ transformation technique are used. The filtered inverter currents i_{ia}, i_{ib}, i_{ic} and grid voltages v_{ga}, v_{gb}, v_{gc} are transformed to the $d-q$ reference frame using the Park transformation matrix, which is expressed as:

$$T = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\theta) & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin(\theta) & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \tag{5}$$

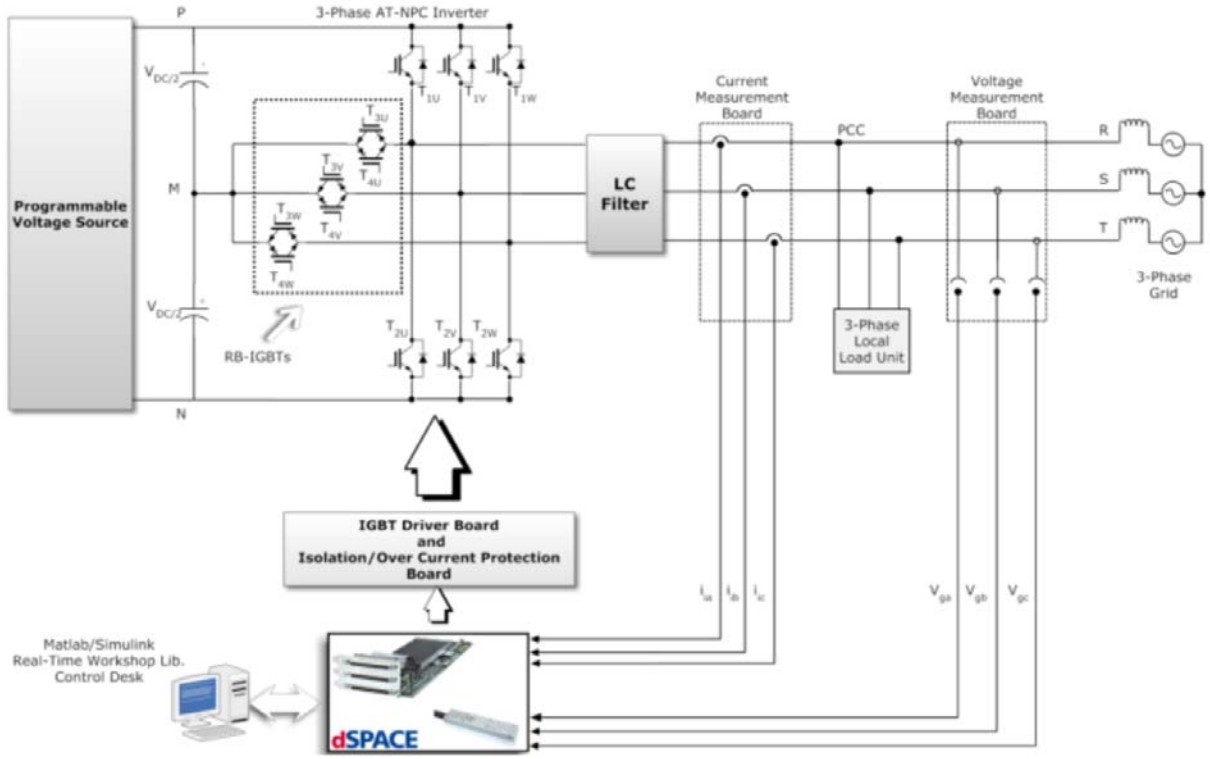


Figure 7. Designed system configuration.

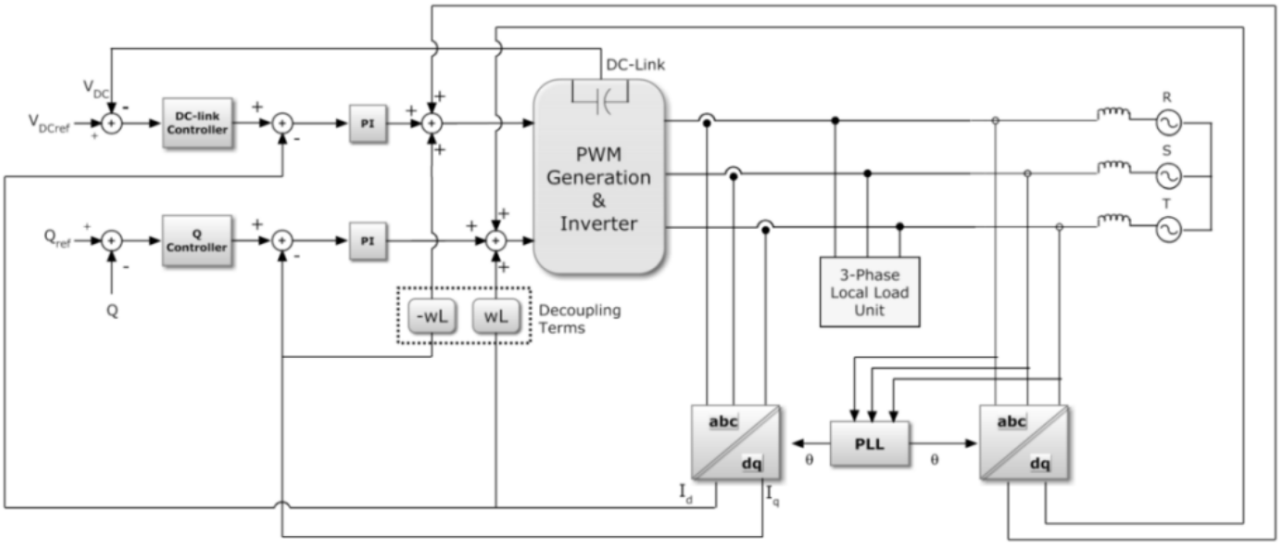


Figure 8. Control block diagram of the system.

where θ is obtained from the PLL algorithm. Transformation to the $d-q$ reference inverter currents and grid voltages are expressed in Eqs. (6) and (7), respectively. After obtaining the $d-q$reference current and voltage, the PI control technique is employed. In this work, the Q-controller reference is set to zero, because there is no need to control reactive power.

$$\begin{bmatrix} I_d \\ I_q \end{bmatrix} = T \begin{bmatrix} i_{ia} \\ i_{ib} \\ i_{ic} \end{bmatrix} \tag{6}$$

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = T \begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \end{bmatrix} \tag{7}$$

In the experimental setup, a 3-phase grid-connected AT-NPC inverter is built with the Fuji Electronics 4MBI300VG-120R-50 module, which includes RB-IGBTs. The system control is achieved digitally using a dSPACE DS1103 controller board. This controller board includes real-time processors and I/O interfaces such as the ± 10 V input voltage level analog-to-digital converter (ADC). With the real-time interface (RTI) of the controller board, the data acquired via ADC and the parameters of the algorithm can be observed graphically in real time. In experiments, inverter currents are measured using LEM LA55P Hall effect-based current sensors, whereas grid voltages are measured using TEG NV25P Hall effect-based voltage sensors. These voltages and currents are scaled to the appropriate voltage level of the dSPACE controller board. PWM signals at the output of the controlled board, which are generated from the control algorithm, are connected to Concept 2SC0108T IGBT drivers [22,23]. The designed inverter power stage is shown in Figure 9.

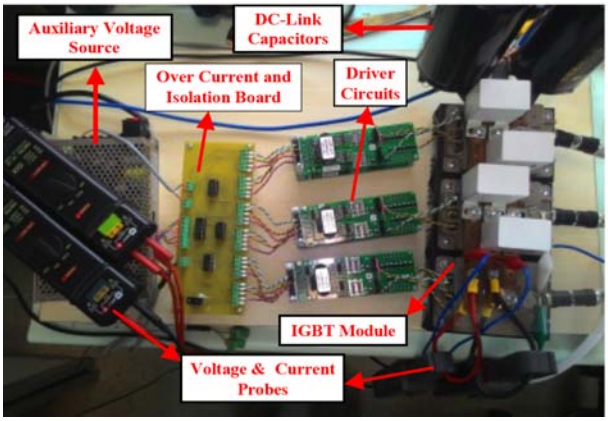


Figure 9. Power stage of the designed 3-phase 3-level AT-NPC-based system.

4. Simulation and experimental results

In order to compare the efficiency of the AT-NPC and T-NPC inverters, simulations are executed using MATLAB/Simulink with PSIM by means of the SimCoupler module. The 1.7-kW AT-NPC and T-NPC inverter power stage is modeled in PSIM, whereas the control system is realized in MATLAB/Simulink. The PSIM simulation block diagram of the AT-NPC inverter is shown in Figure 10 and the MATLAB/Simulink schematic of the control system is shown in Figure 11. As shown in Figure 11, the SimCoupler block in MATLAB/Simulink is properly linked to the PSIM schematic of the AT-NPC inverter.

To calculate the switch losses in the simulation, the Fuji Electric 12MBI50VN-120-50 (with RB-IGBT) module, existing in the PSIM's Thermal Module device database, is used in the AT-NPC inverter power stage. The module contains 1200-V, 50-A normal IGBTs and 600-V, 50-A RB-IGBTs. In the T-NPC inverter power stage, only bidirectional switches at the midpoint leg are replaced by a common emitter series connection of

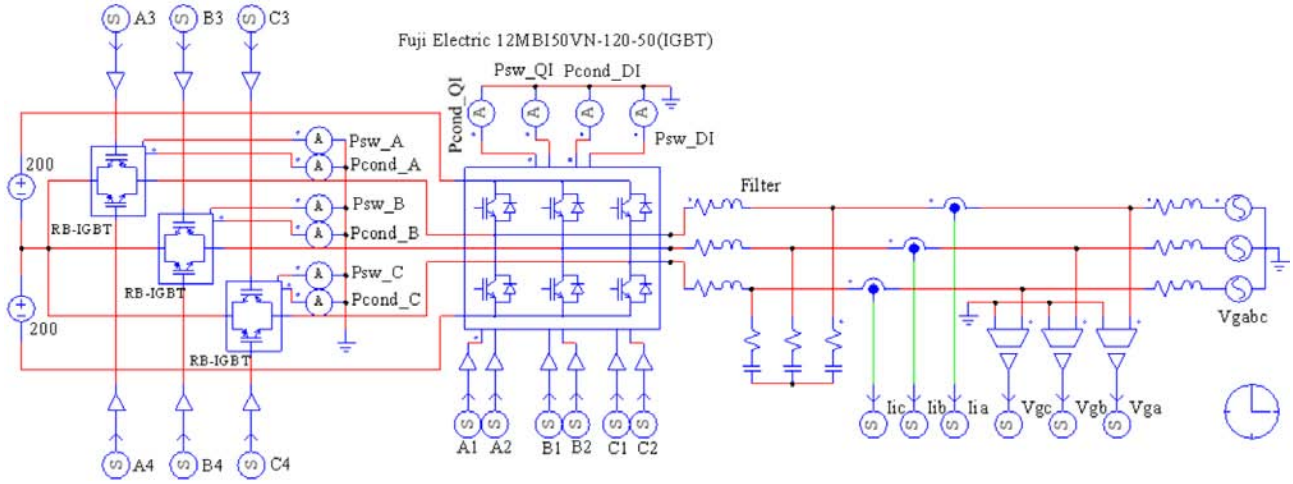


Figure 10. Simulation block diagram of the AT-NPC inverter in PSIM.

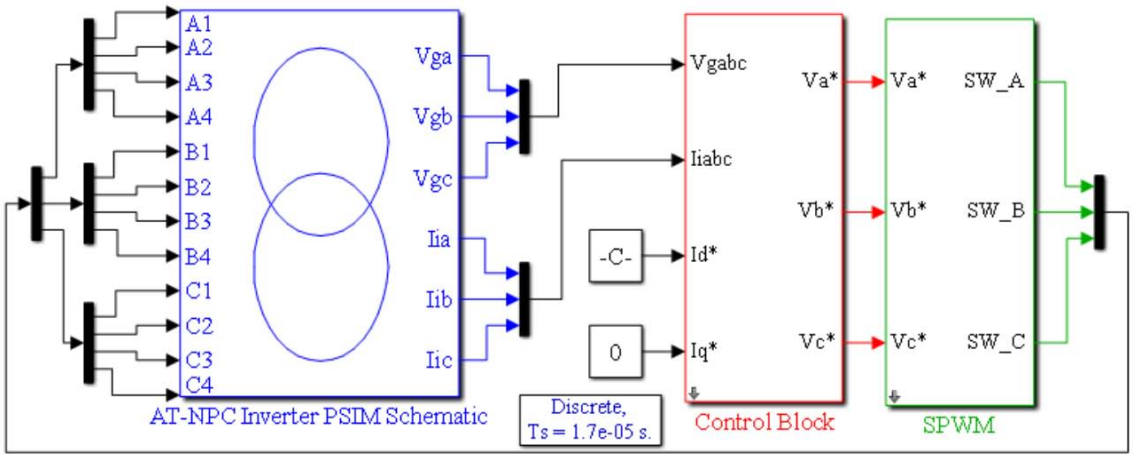


Figure 11. Schematic of the control system in MATLAB/Simulink.

two Fairchild Semiconductor HGTG20N60A4D modules. The module, existing in the PSIM device database, includes 600-V and 40-A normal IGBTs with an antiparallel diode.

The simulation results of the conduction and switching loss waveforms for the AT-NPC and T-NPC inverters are shown in Figures 12a and 12b, respectively. The switching and conduction losses are 17.8 W and 8.6 W for the AT-NPC inverter, whereas these losses are 35.3 W and 8.1 W for the T-NPC inverter, respectively. Additionally, the efficiency of the AT-NPC inverter is 98.4% and that of the T-NPC inverter is 97.4%. As a result, the AT-NPC inverter has lower total switch losses than the T-NPC inverter at the same switching frequency (5 kHz).

In the experimental study, the currents and voltages are measured with Fluke 80i-110s current probes and Pintek DP-25 differential probes with a Tektronix DPO 3054 four-channel digital oscilloscope. The power losses of switching devices are evaluated with the DPO3PWR power analysis application module installed on the oscilloscope, and the power analysis of the experimental measurements is realized with the Fluke 434 power quality analyzer. The designed system parameters are summarized in Table 3.

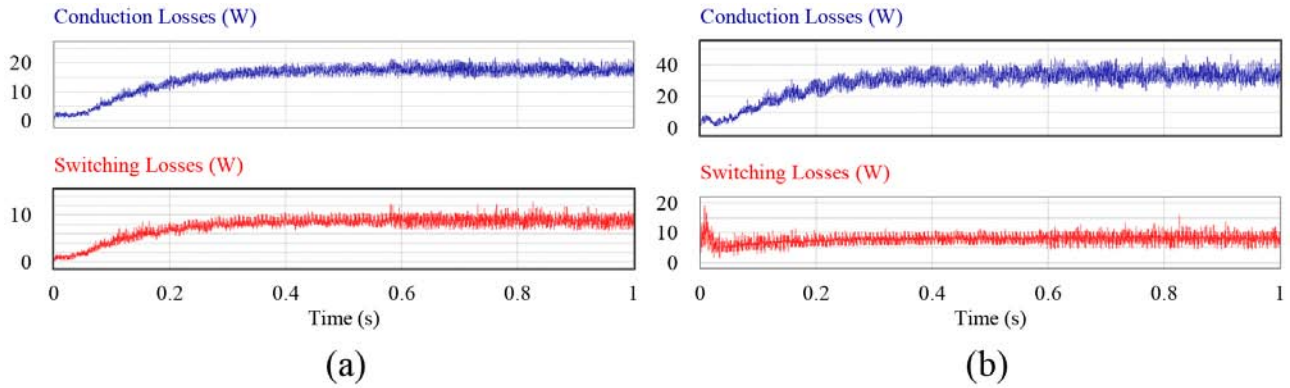


Figure 12. Conduction and switching loss waveforms of (a) AT-NPC, (b) T-NPC inverter.

Table 3. Proposed system parameters.

Parameters	Values
Grid voltage and frequency	110 V, 50 Hz
DC-link voltage	400 V
Filter inductance	8.9 mH
Filter capacitor and damping resistor	30 μF, 10 Ω
Load unit per phase	121 W
Switching frequency	5 kHz

The simulation model of the 3-level AT-NPC inverter control strategy is designed in MATLAB/Simulink. This model is then automatically compiled and downloaded to dSPACE DS1103 real-time hardware. Additionally, 3-phase grid voltages, 3-level inverter currents, and PLL block output are monitored, and PI controller parameters are adjusted online with real-time simulation using dSPACE ControlDesk software, as shown in Figure 13. Thus, the control system performance is improved by this software. The phase-to-phase output voltage of the inverter is shown in Figure 14. The 3-level inverter output currents and their harmonic values are shown in Figure 15. As shown in Figure 15a, the 3-level AT-NPC inverter currents are sinusoidal waveforms. Furthermore, the THD values of these currents are close to the IEEE 519 harmonic limit value of 5%, as shown in Figure 15b.

Experimental waveforms of grid voltage, grid current, inverter current, and load current are acquired as shown in Figure 16. The DC current supplied by the programmable voltage source is converted into grid-voltage synchronized AC current at the inverter output. This current is divided into two directions at the PCC. After the current requirement of the load unit is supplied, the remaining part of the inverter current is transferred to the grid. In the DC side of the inverter, the programmable voltage source is employed with approximately 400.1 V and 4.23 A values; thus, the absorbed DC power is about 1.7 kW. The experimental power and energy values of the load unit, inverter, and grid are indicated in Figures 17a–17c, respectively. It can be seen from these figures that the output current of the inverter is 4.8 A; 1.1 A of this current is delivered to the load, and the remaining 3.7 A of the inverter current is transferred to the grid. The switching waveforms of T3 and T1 are given in Figures 18a and 18b, respectively. In this study, Eqs. (1)–(4) are used with the switching waveforms for the calculation of switch losses. The calculated switch losses of the 3-phase AT-NPC inverter are detailed in Figure 19. As shown in Figure 19a, total switch loss power of the twelve switches is 63.11 W, as illustrated in Figure 19b. The switch losses power percentage of the inverter power is about 3.7%.

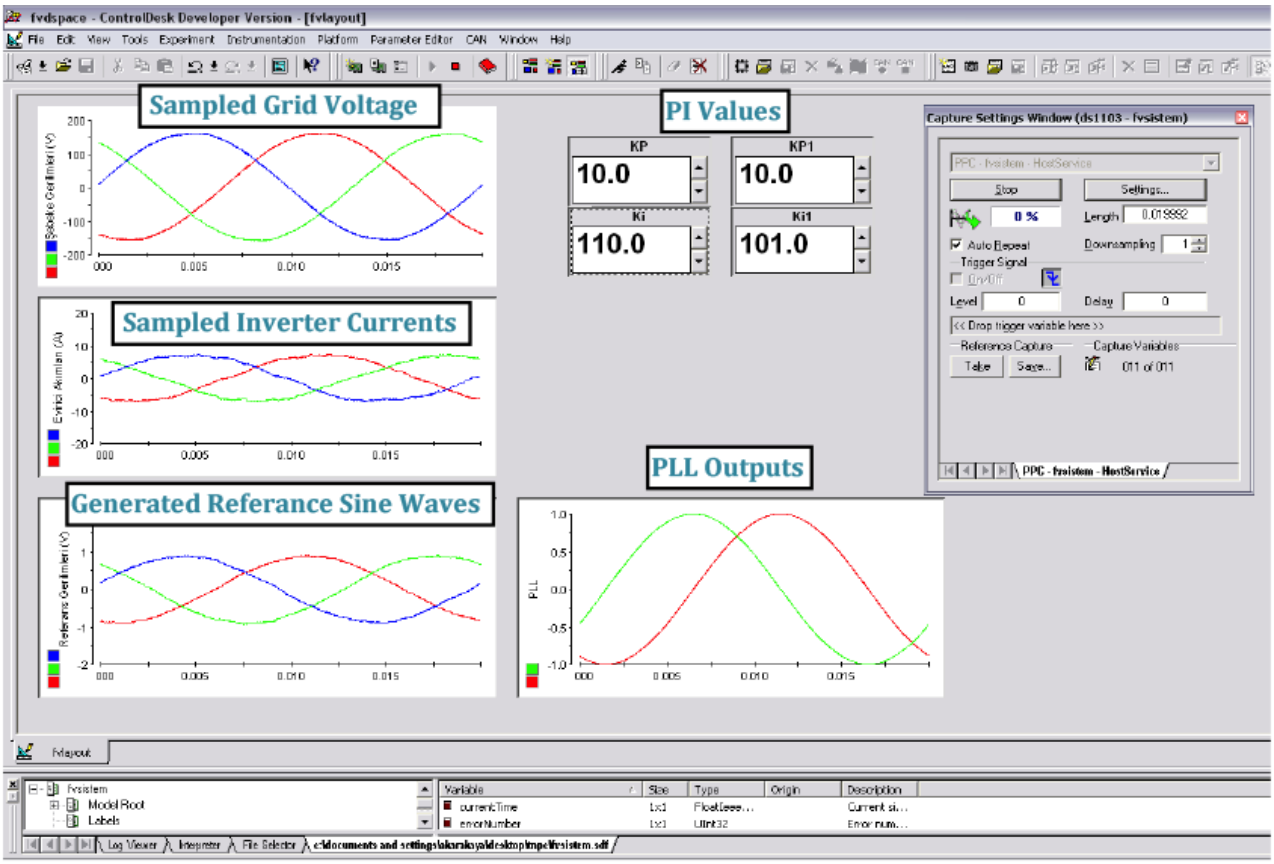


Figure 13. ControlDesk interface for the proposed system.

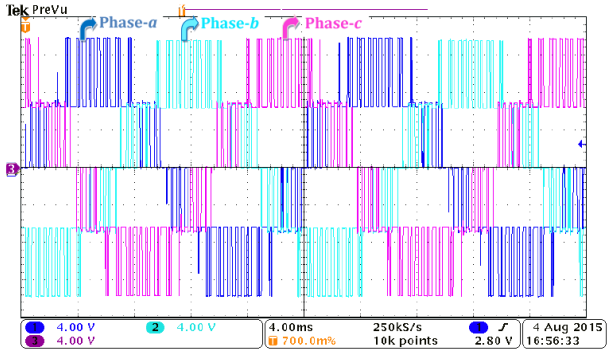


Figure 14. Phase-to-phase output voltage of the inverter.

5. Conclusion

This study presents the analysis, design, and control of a 3-phase 3-level grid-connected AT-NPC inverter for low-voltage applications. The AT-NPC topology, which is a newly developed T-NPC topology, has been realized by using the highly efficient RB-IGBT on the bidirectional switch in the middle leg. In this work, competitive analyses of the proposed grid-connected inverter have been performed with 2-level, classical NPC, and T-NPC inverters. Additionally, switching configurations are detailed for experimental operation principles. The experimental setup of the proposed 3-phase grid-connected inverter, based on dSPACE DS1103 real-time

hardware, has been built in order to verify the improvement of the conversion efficiency. The experimental results confirm that the proposed inverter, with an efficiency of 96.3%, is a good alternative to grid-connected inverters requiring high efficiency in low-voltage applications.

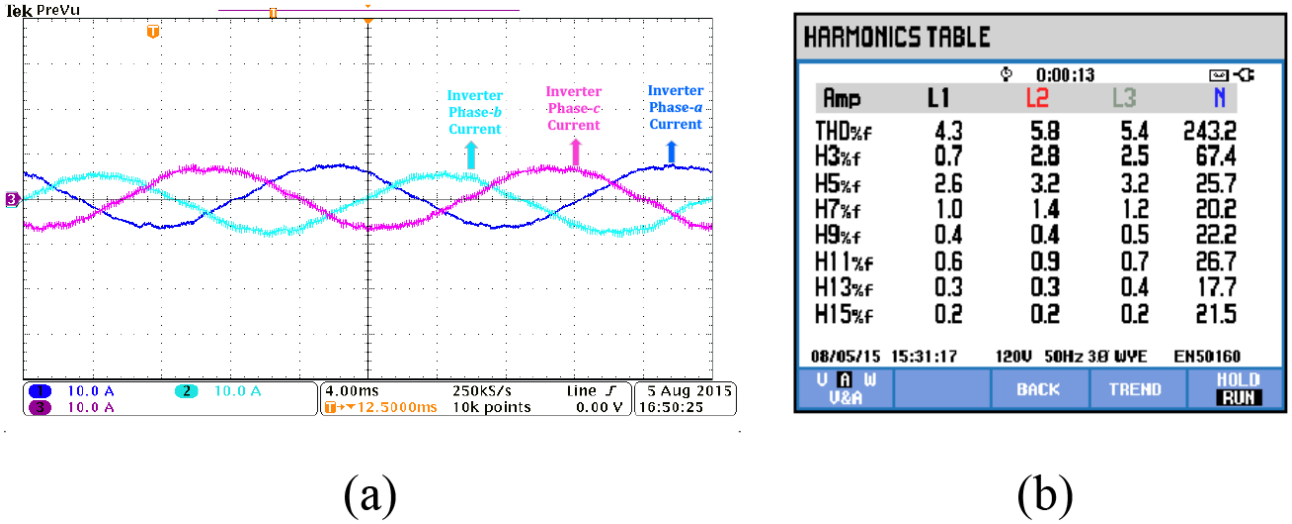


Figure 15. (a) Inverter output currents, (b) harmonic values.

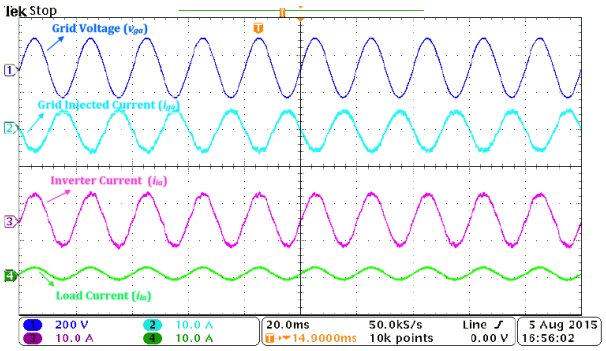


Figure 16. Voltage and current waveforms at PCC.

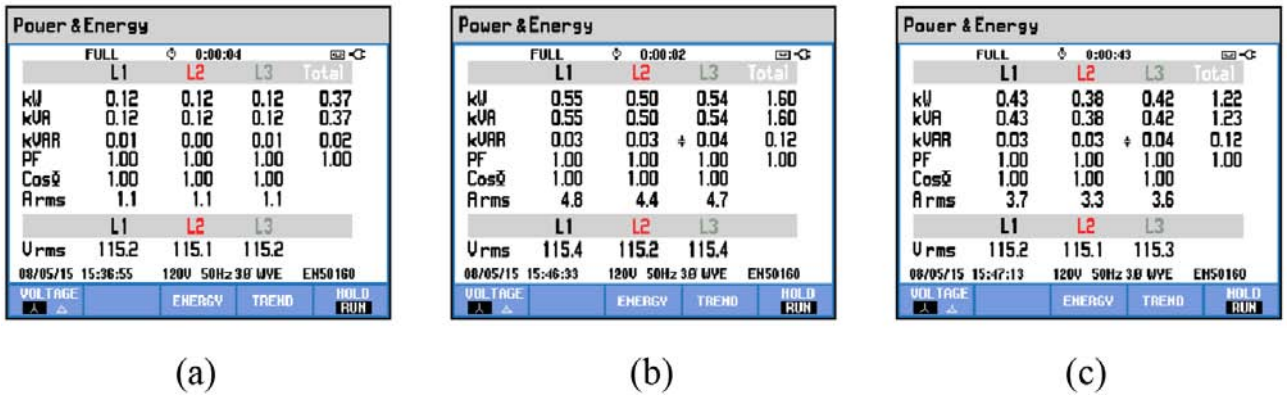


Figure 17. Power and energy values for the (a) load, (b) inverter, (c) grid.

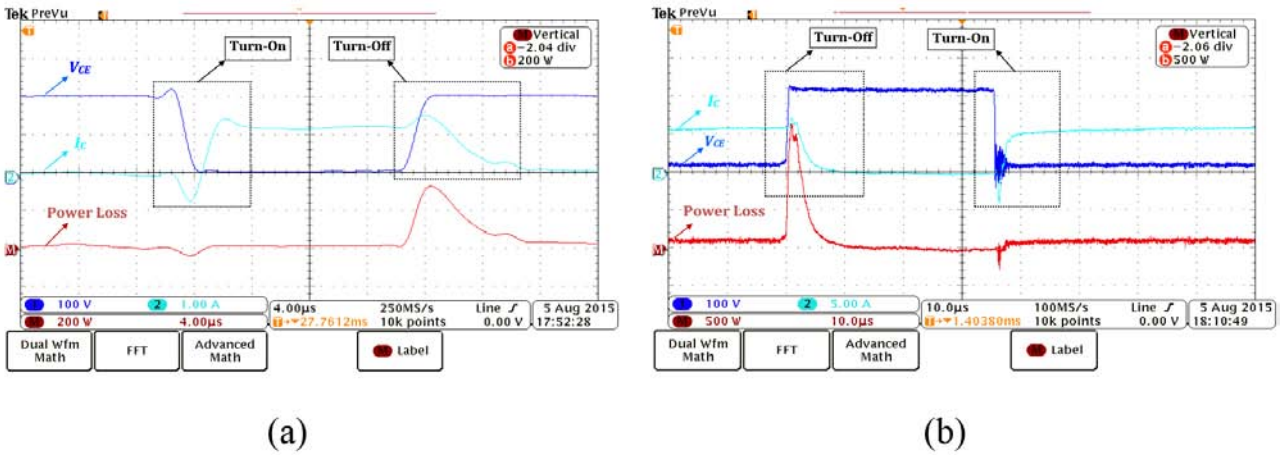


Figure 18. Switching waveform of (a) T3, (b) T1.

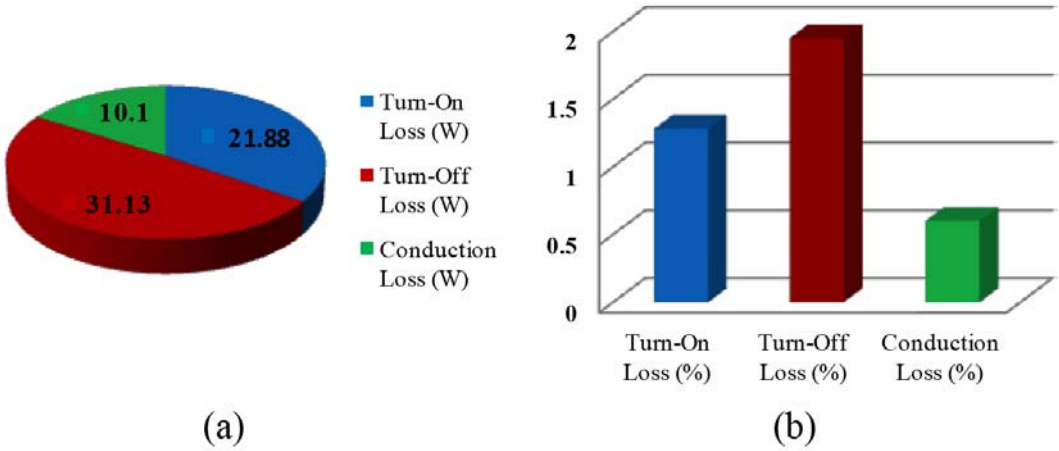


Figure 19. (a) Switch losses, (b) power losses percentage of the inverter power.

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