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INVESTIGATION WITH TCSC, SSSC AND UPFC OF STATIC VOLTAGE STABILITY IN ZIP LOAD MODELING

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Abstract

Voltage stability refers to the ability of a power system to maintain steady voltages at all buses in the system after being subjected to a disturbance from a given initial operating condition. One of the conditions affecting the voltage stability is the nonlinear load model. Maximum loading parameter-voltage in power systems of the nonlinear load modeling relation is important for static voltage stability. In this study, the effects on static voltage stability of static impedance, current, and active power (ZIP) load modeling in 5 bus power system are investigated. As maximum load analysis, Thyristor Controller Series Compensator (TCSC) Static Synchronous Seri Compensator (SSSC) and Unified Power Flow Controller (UPFC) from Flexible AC Transmission System (FACTS) devices are used. The impacts of ZIP load modeling on different parameter values were evaluated in terms of voltage-maximum loading parameters. Besides, voltage profile of 5 buses power system with TCSC, SSSC and UPFC in different parameter values was examined. Particularly, with use of UPFC has shown that static voltage stability is more effective and maximum load parameter value is increased.

Keywords: ZIP Load Modeling, Maximum Loading Parameter, TCSC, SSSC, UPFC

ZIP YÜK MODELİNDE STATİK GERİLİM KARARLILIĞININ TCSC, SSSC VE UPFC İLE İNCELENMESİ

Öz

Gerilim kararlılığı, bir güç sisteminin belirli bir ilk çalışma koşulundan kaynaklanan bir bozunuma maruz kaldıktan sonra sistemdeki tüm baralarda sürekli gerilimi tutabilme yeteneğini ifade eder. Gerilim kararlılığını etkileyen durumlardan birisi lineer olmayan yük modelidir. Lineer olmayan yük modellerinin güç sistemlerinde maksimum yüklenme parametresi-gerilim ilişkisi statik gerilim kararlılığı için çok önemlidir. Bu çalışmada 5 baralı güç sisteminde sabit empedans, akım ve aktif güç (ZIP) yük modelinin statik gerilim kararlılığında oluşturmuş olduğu etkiler incelenmiştir. Maksimum yüklenme analizi için güç sisteminde Esnek AC İletim Sistemi (FACTS) elemanlarından Tristör Kontrollü Seri Kompanzatör (TCSC), Statik Senkron Seri Kompanzatör (SSSC) ve Birleştirilmiş Güç Akışı Kontrolü (UPFC) kullanılmıştır. ZIP yük modelinin farklı parametre değerindeki etkileri gerilim-maksimum yüklenme parametresi açısından yorumlanmıştır. Dahası farklı parametre değerlerinde TCSC, SSSC ve UPFC ile 5 baralı güç sisteminin gerilim profilleri incelenmiştir. Özellikle UPFC'nin kullanılması ile statik gerilim kararlılığında daha etkili olduğu ve maksimum yüklenme parametre değerinin arttığı görülmüştür.

Anahtar Kelimeler: ZIP Yük Modeli, Maksimum Yüklenme Parametresi, TCSC, SSSC, UPFC

Cite

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1. Introduction

Due to the complexity of power systems and the constant changes in the demand for customers, stability problems have arisen. One of the most important of the problems of stability is voltage stability occurring depending on loading. Generally, voltage stability determines as relationship between loading and voltage profile in the load bus. There are studies in literature related to voltage stability. In infinite power systems and multi-machine power systems, transmission line length changes, power factor changes, line head voltage change, line loss factor participation, differences in parallel line number used, and different shunt and series compensation ratio changes are analyzed for static voltage stability [1]. Among the factors that cause voltage stability problems have seen in line break out and faults. In conditions line break out and faults in bus, Relations between bus voltage-active powers are investigated. Stability and instability operating regions of the power systems are interpreted [2-5]. In another voltage stability analysis, the effects of different transformer phase shift ratios and different step change ratios in the IEEE 14-bus power system have been investigated. The relationship between the bus voltage and the maximum load parameter in

different phase shifting and tap changer ratios has been investigated. Both conditions were found to have an effect on the voltage stability [6-7]. The effects of load and voltage changes on the system in power systems using 3 wound transformers are also investigated. Once the three-winding transformer reactance are different, the operating conditions are discussed [8]. Flexible AC Transmission System (FACTS) devices are commonly used to increase the operating limits of the bus voltage and to keep the maximum loading-voltage values stable in power systems. Static Synchronous Compensator (STATCOM), Static Var Compensator (SVC), Static Synchronous Serial Compensator (SSSC), Thyristor Controlled Serial Compensator (TCSC) and Unified Power Flow Controller (UPFC) from FACTS devices have been increased in maximum loading parameter value. Therefore, FACTS devices can be improved to operation limits of the power systems [9-12].

In this study, with ZIP load model used with the second order equation occurring constant impedance, constant current and constant active power (ZIP), relation between maximum loading parameter of the 5 bus power system are investigated with TCSC, SSSC and UPFC. Effect of the FACTS devices connected as series transmission line of the parameter changes in the ZIP load model are also examined. It is seen that UPFC used as a converter based gives better results than other series FACTS devices.

2. Static Voltage Stability and Continuous Power Flow

Static voltage stability depends on reactive power change. The operating conditions of the load bus can be improved by providing reactive power. If the reactive power support decrease below the specified limits and the voltage drop, the system break-out arises. To prevent this problem, different operation modes is enhanced for static voltage stability. The relation between the system maximum-load parameter and the active power-reactive power of the bus are shown in Eq. 1 and Eq. 2.

$$P_L = P_{L0}(1+\lambda) \quad (1)$$

$$Q_L = Q_{L0}(1+\lambda) \quad (2)$$

PL0 and QL0, are initial active and reactive power values, PL and QL are active and reactive power of the load λ maximum loading parameter value, respectively. In the continuous load flow, the relationship between the voltage and the maximum load parameter is used. Continuous load flow method is used for the analysis of voltage and MLP. Continuous load flow is very effective in analyzing certain difficulties without the support of certain system models. The voltage has the ability to automatically change against the adverse situation that may be caused by single analysis of the system equations. The use of strategy in continuous load flow is shown in Fig. 1.

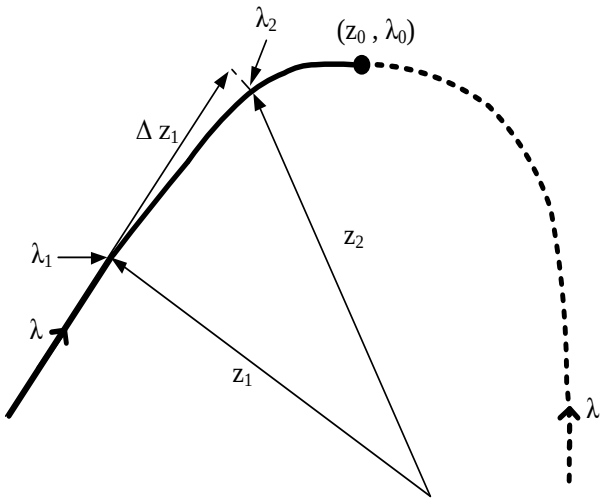

Figure 1. Continuous power flow method

Here, (z1, λ1) is known as balance point, Δλ1is used for parameter value change and Δz1 is used for vector analysis. At the first stage, prediction is done. z1+ Δz1+ Δλ1 values are produced initially. These values are used for correcting z2 +Δz2 which are the new balance points in the system profile [12].

3. ZIP Load Modeling

The static load characteristic is the load model classified as constant impedance, constant current and constant active power depending on the voltage. For a constant impedance load, there is a second order equation depending on the active-reactive power. It is completely independent of the power-voltage variation when the constant current is linear and power. ZIP load model active and reactive power equations are given in Eq. 3 and Eq. 4.

$$P = P_0\left[p_1\left(\frac{V}{V_0}\right)^2 + p_2\frac{V}{V_0} + p_3\right] \quad (3)$$

$$Q = Q_0\left[q_1\left(\frac{V}{V_0}\right)^2 + q_2\frac{V}{V_0} + q_3\right] \quad (4)$$

Where p1 and q1 are the constant impedance load parameters, p2 and q2 are the constant current load parameters, and p3 and q3 are the constant power load parameters. p1 +p2 +p3 = 1 and q1 + q2 + q3 = 1 when V = V0. ZIP load model circuit model is given in Fig. 2 [13].

ZIP load model consists of d-q axis transformation, variable frequency average value Phase-locked loops (PLL) and active and reactive power calculation circuit.

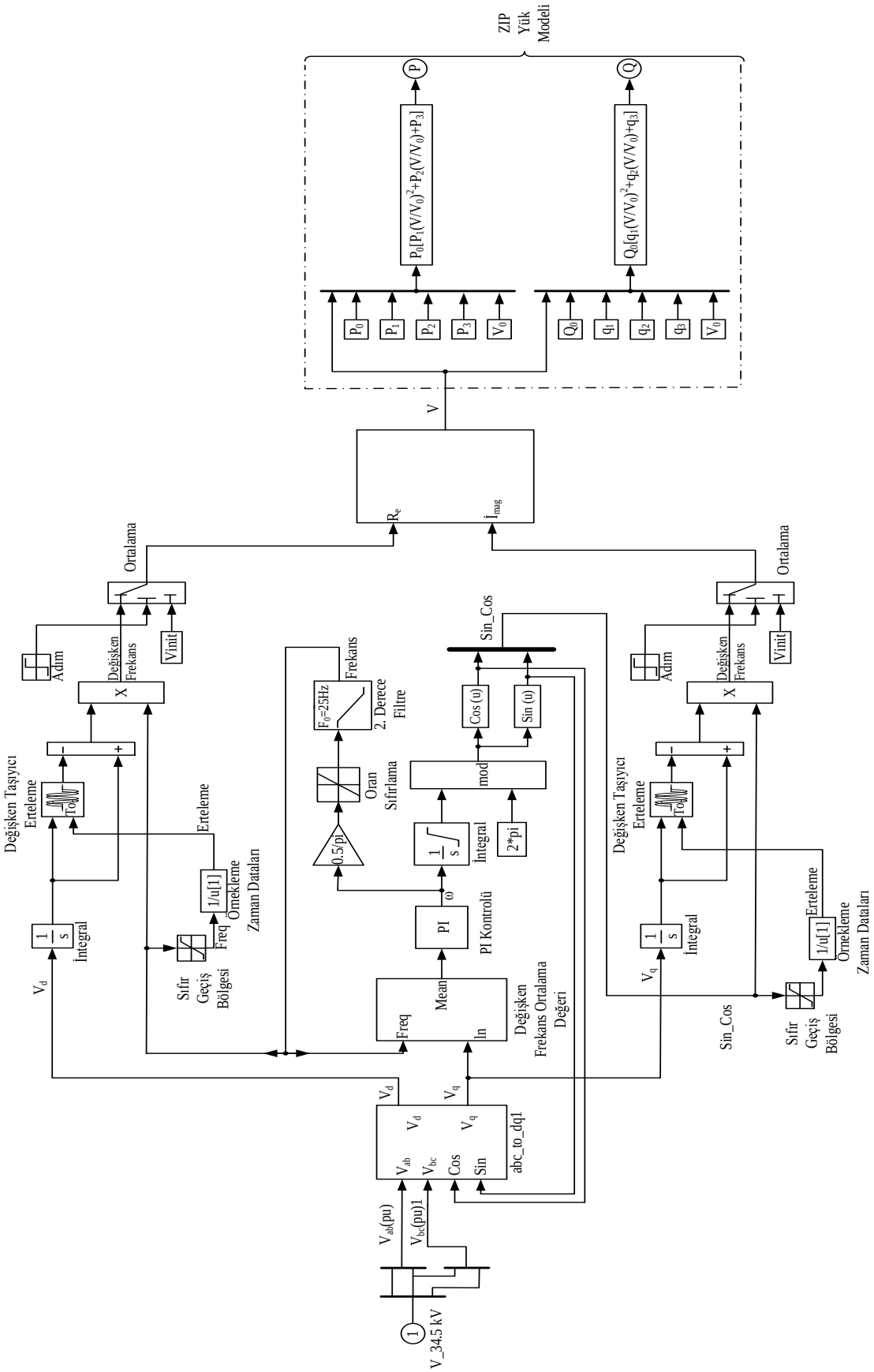

Figure 2. ZIP load model.

4. TCSC, SSSC ve UPFC Modeling

Thyristor Controller Series Compensator (TCSC) is connected to transmission line in series and consist of Thyristor Controller Reactor (TCR) and Thyristor Switched Capacitor (TSC). Generally, TCSC is used for the aim to current control in transmission lines. TCSC control and circuit model are seen in Fig. 3.

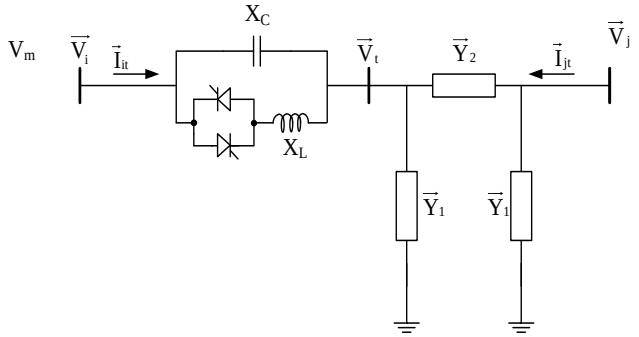

Figure 3. TCSC circuit model.

The difference between reference current and measured current value is considered by unit of controller triggering angles of thyristors are determined. With these triggering angles, the inductive and capacitive operating modes of the TCSC have been set. Control equations in TCSC are given between Eq. 5 and Eq. 9.

The difference between reference current and measured current value is considered by unit of controller triggering angles of thyristors are determined. With these triggering angles, the inductive and capacitive operating modes of the TCSC have been set. Control equations in TCSC are given between Eq. 5 and Eq. 9.

$$P + V_i V_j B_e \sin(\delta_i - \delta_j) = 0 \quad (5)$$

$$-V_i^2 B_e + V_i V_j B_e \cos(\delta_i - \delta_j) - Q_i = 0 \quad (6)$$

$$-V_j^2 B_e + V_i V_j B_e \cos(\delta_i - \delta_j) - Q_j = 0 \quad (7)$$

$$B_e - B_e(\alpha) = 0 \quad (8)$$

$$P + jQ_i - IV_i = 0 \quad (9)$$

Where, P active power, Vi i bus voltage, Vj j bus voltage, Be suseptance, δi i bus voltage angle, δj j bus voltage angle, Qi i bus reactive power, I measurement current, Be (α) thyristor depend new suseptance. TCSC current and admittance equation are shown in Eq. 10 and Eq. 11.

$$I_{it} = \frac{Y_{TCSC}(Y_i + Y_j)V_i - Y_i V_j}{Y_{TCSC} + Y_i + Y_j} \quad (10)$$

$$Y_{TCSC} = \frac{1}{jX_{TCSC}} \quad (11)$$

Static Synchronous Series Compensator (SSSC) is consist of voltage source converter (VSC) circuit which is connected series to the transmission line. Current control of transmission line provided by DC link voltage. SSSC circuit model are shown in Fig. 4.

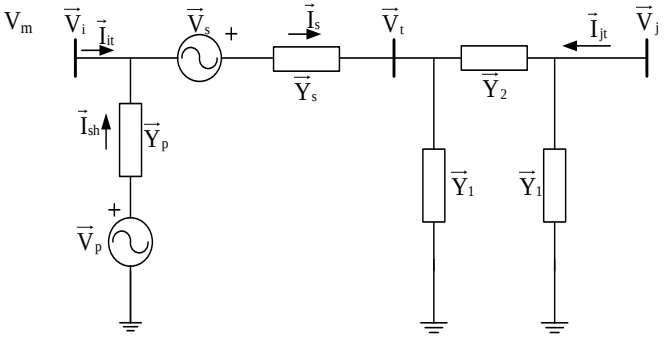

Figure 4. SSSC circuit model.

The difference between reference current Vdc and measured current Vdcref value is considered by unit of controller triggering angles of thyristors are determined. SSSC control equations are given between Eq. 12 and Eq. 14.

$$I - I_{ref} = 0 \quad (12)$$

$$V_{dc} - V_{dcref} = 0 \quad (13)$$

$$P - V_{dc}^2 / RC - RI^2 = 0 \quad (14)$$

1. where, I measurement current, Iref reference current, Vdc DC link voltage, Vdcref reference DC voltage, P active power, C capacitor, R resistance. SSSC current and admittance equations are shown in Eq. 15 and Eq. 16.

$$I_{it} = \frac{Y_{SSSC}(Y_i + Y_j)V_i - Y_i V_j}{Y_{SSSC} + Y_i + Y_j} \quad (15)$$

$$Y_{TCSC,SSSC} = \frac{1}{jX_{SSSC}} \quad (16)$$

UPFC is a FACTS device that is connected both in series and in parallel to the transmission line. Generally, UPFC is consist of combination of STATCOM and SSSC. While STATCOM provides to voltage control of the bus, SSSC provides to current control of the transmission line. UPFC circuit model are shown in Fig. 5.

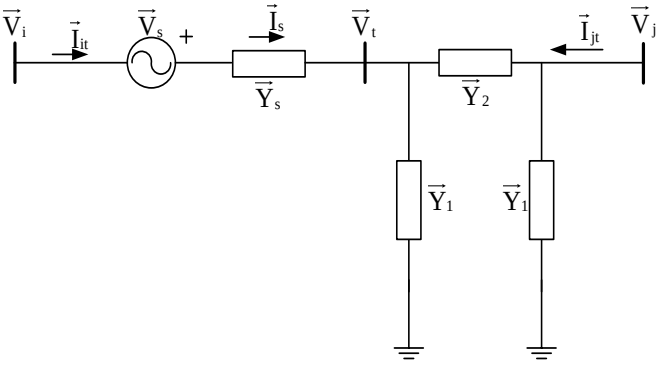

Figure 5. UPFC circuit model.

The current and the voltage control in the bus and transmission line are provided by the DC link unit. Trigger angles of the thyristor are calculated in the converter circuit according to the current and voltage values in the DC link unit. UPFC control equation are shown between Eq. 17 and Eq. 20 [14].

$$I - I_{ref} = 0 \quad (17)$$

$$V_{dc} - V_{dcref} = 0 \quad (18)$$

$$P - V_{dc}^2 / RC - RI^2 = 0 \quad (19)$$

$$V_t = \frac{Y_s(V_i + V_s) + Y_1 V_j}{Y_s + Y_1 + Y_2} \quad (20)$$

5. Simulation Model and Results

5.1. Simulation Model

5 buses power system model is given in Fig. 6.

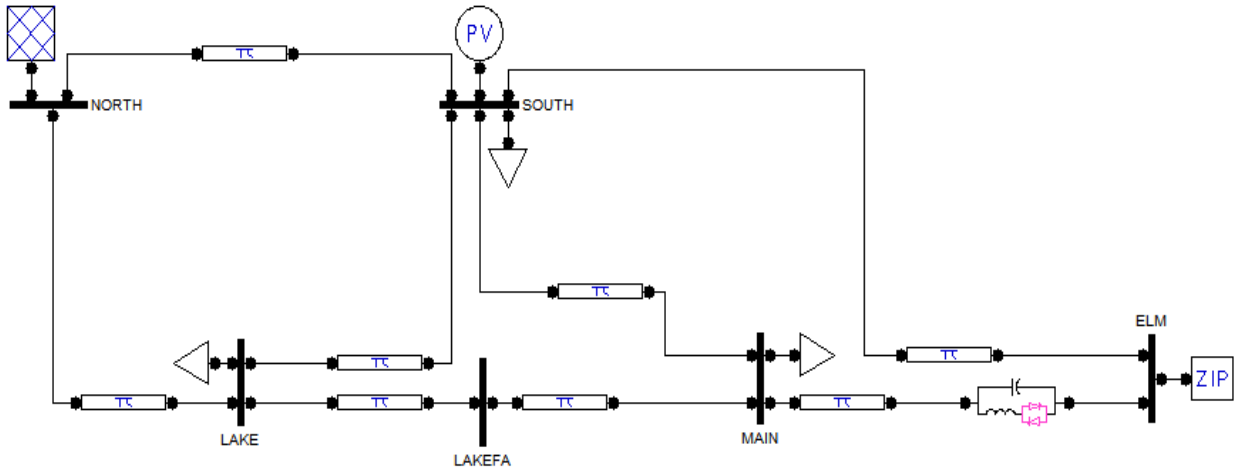

Figure 6. 5 buses power system

A modeling and simulation study has been carried out on 11 buses power system [15-16]. 5 bus test system is shown in Fig. 3. The system occurs form 1 slack bus, 3 load buses, and 1 generator bus.

5.2. Simulation Model Results

ZIP load model is used connected to instead of the PQ bus load model with the lowest voltage profile. With ZIP load input parameters are regulated to different values, Maximum loading parameter value is calculated.

When both ZIP load active power and ZIP load reactive power input parameters with TCSC used in test system are used as 0.05-0.05-0.9, 0.1-0.1-0.8 and 0.15-0.15-0.7, the maximum load parameter of the system 1.95, 2.09 and 2.25, respectively. The relationship between voltage-maximum loading parameter with TCSC is shown in Fig. 7, Fig. 8 and Fig. 9.

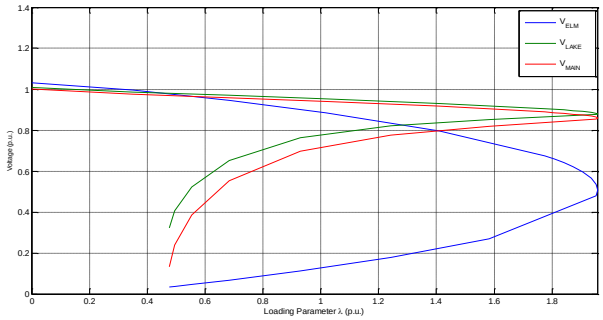

Figure 7. Voltage-MLP curves in 0.05-0.05-0.9 value with TCSC (1.95).

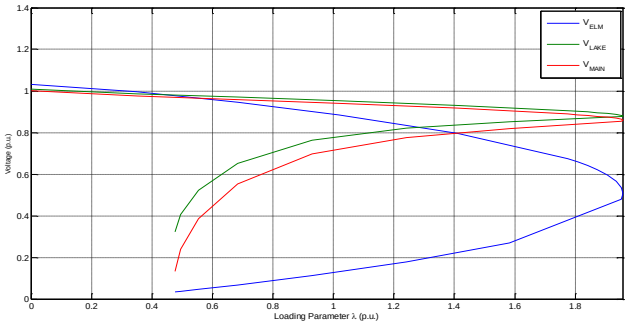

Figure 8. Voltage-MLP curves in 0.1-0.1-0.8 value with TCSC (2.09).

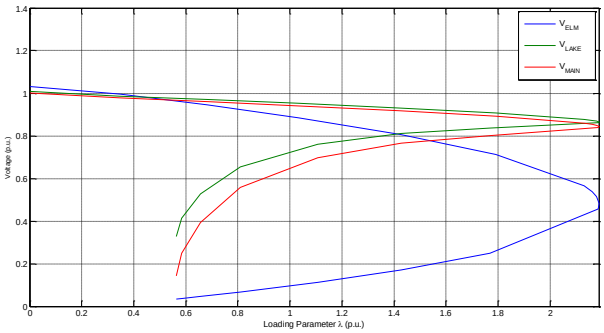

Figure 9. Voltage-MLP curves in 0.15-0.15-0.7 value with TCSC (2.25).

When both ZIP load active power and ZIP load reactive power input parameters with SSSC used in test system are used as 0.05-0.05-0.9, 0.1-0.1-0.8 and 0.15-0.15-0.7, the maximum load parameter of the system 2.37, 2.56 and 2.75, respectively. The relationship between voltage-maximum loading parameter with SSSC is shown in Fig. 10, Fig. 11 and Fig. 12.

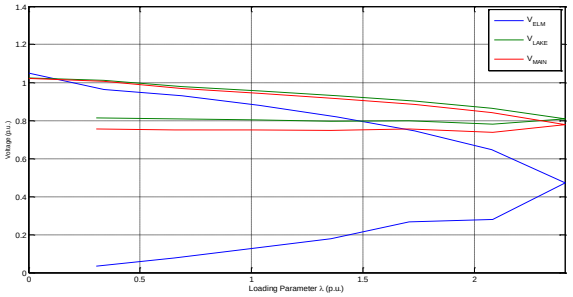

Figure 10. Voltage-MLP curves in 0.05-0.05-0.9 value with SSSC (2.37).

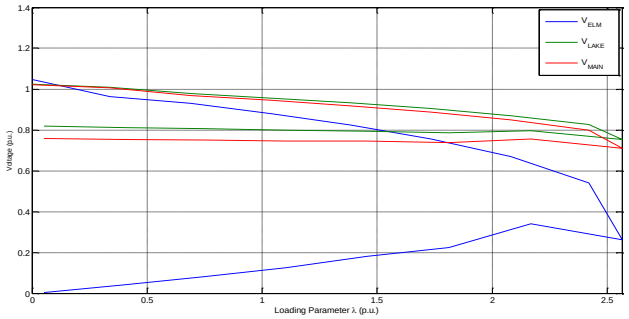

Figure 11. Voltage-MLP curves in 0.1-0.1-0.8 value with SSSC (2.56).

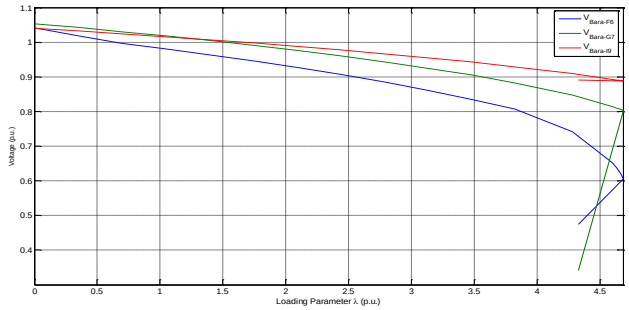

Figure 12. Voltage-MLP curves in 0.15-0.15-0.7 value with SSSC (2.75).

When both ZIP load active power and ZIP load reactive power input parameters with UPFC used in test system are used as 0.05-0.05-0.9, 0.1-0.1-0.8 and 0.15-0.15-0.7, the maximum load parameter of the system 3.25, 3.49 and 3.73, respectively. The relationship between voltage-maximum loading parameter with SSSC is shown in Fig. 13, Fig. 14 and Fig. 15.

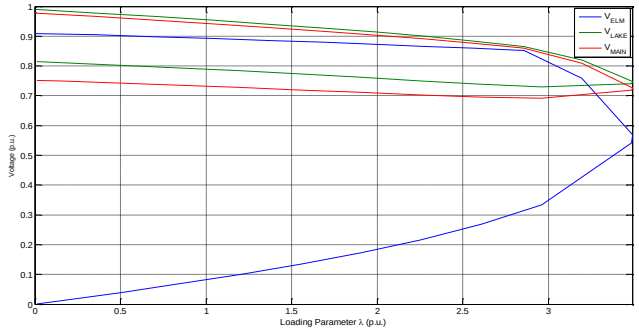

Figure 13. Voltage-MLP curves in 0.05-0.05-0.9 value with UPFC (3.25).

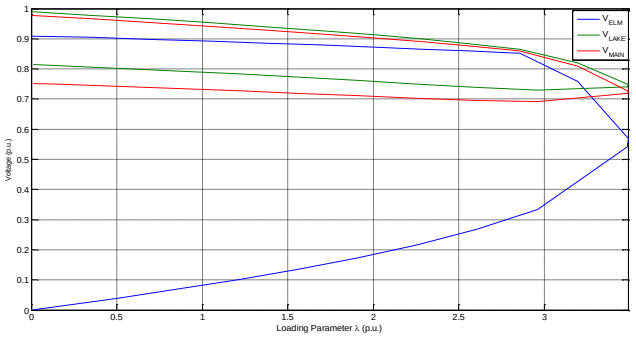

Figure 14. Voltage-MLP curves in 0.1-0.1-0.8 value with UPFC (3.49).

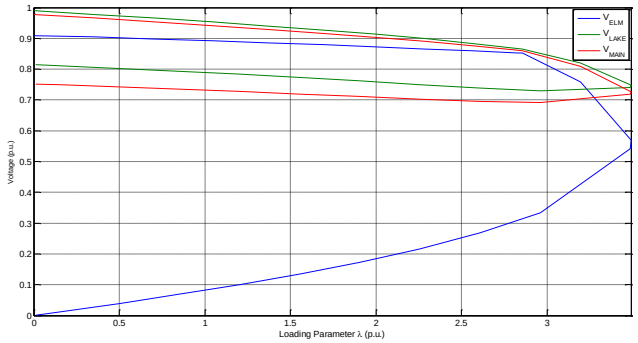

Figure 15. Voltage-MLP curves in 0.15-0.15-0.7 value with UPFC (3.73).

6. Conclusions

In this study, static voltage stability analysis in different load parameter values of ZIP load model were examined with TCSC, SSSC and UPFC from FACTS devices. TCSC, SSSC and UPFC has been increased in different parameter values maximum loading parameter of the 5 buses power system. Especially UPFC, which is a power electronic based compensation device, has higher voltage-maximum load parameter value than TCSC and SSSC. With the use of STATCOM in the ZIP load model, the maximum load parameter value very little changes as the load parameters change. However, with use of UPFC in ZIP load model, the maximum loading parameter changes to a greater extent. The highest loading value was obtained by using the STATCOM and ZIP load model at 0.15-0.15-0.7 value. This maximum loading parameter value is 3.73. The smallest loading value was obtained by using the TCSC and ZIP load model at 0.05-0.05-0.9 value. This maximum loading parameter value is 1.95. The effect of the ZIP load model with FACTS devices used in 5 buses power system was found to be significant on the voltage stability.

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