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Proportional multi-resonant-based controller design method enhanced with a lead compensator for stand-alone mode three-level three-phase four-leg advanced T-NPC inverter system

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Abstract: This study presents an inverter current sampled double-loop proportional multi-resonant (PMR)-based control technique for three-level (3L) three-phase four-leg (3P4L) advanced T-type neutral point clamped (AT-NPC) stand-alone mode inverter. Apart from the conventional linear controller the PMR controller has the ability to track a sinusoidal reference and does not require any axis transformation. Therefore, the main advantage of the proposed control technique for a 3P4L inverter is to independently control the output phase voltages when feeding a single phase and/or three phase loads. This is achieved by the inverter current sampled double-loop controller with a lead compensator in order to increase the control system phase margin unlike the capacitor current sampled controller. Thus, the harmonic compensation capability of the controller is increased which strengthens the controller against highly non-linear load types. The design procedures of the controller for the system are analytically explained. Then, the steady-state and dynamic performance of the controller is tested in a 3L 3P4L AT-NPC inverter system through many simulations and experimental studies. The results verify the fast-dynamic performance and the achievement of the low total harmonic distortion with a maximum of 2.89% for the 3L 3P4L AT-NPC inverter system even under serious non-linear load type.

Nomenclature

v_{inv}	inverter output voltage
L_a, L_b, L_c	filter inductor of each phase
C_a, C_b, C_c	filter capacitor of each phase
r_a, r_b, r_c	equivalent series resistances of each phase filter inductor
V_A, V_B, V_C	inverter voltages after filtering (see Fig. 1)
I_{L}	filter inductor current
v_{fn}	offset voltage
v_{af}^*, v_{bf}^*, v_{cf}^*	phase reference voltages
v_{min}^*	minimum value of the phase reference voltages
v_{max}^*	maximum value of the phase reference voltages
K_{CC}	proportional part of the inner loop
$G_{\text{CC}}(s)$	closed loop transfer function of the inner loop
K_{PWM}	PWM gain
f_{c}	cross-over frequency
ζ	damping coefficient of the outer loop controller
w_{bw}	desired bandwidth frequency of the controller
f_{sw}	switching frequency
$v_{\text{out}}(s)/v_{\text{ref}}(s)$	system transfer function
K_{VC}	proportional part of the outer loop
h	harmonic order
K_{ih}	integrator gain of each harmonic
ω_{ch}	cut-off frequency of each harmonic
ω_h	resonant frequency of each harmonic
f_{co}	crossover frequency
T_{PWM}	PWM update delay time
T_{samp}	digital sampling delay time
T_{comp}	computation delay time
T_{d}	total time delay
Φ_{max}	maximum phase margin of the lead compensator
w_{m}	maximum phase margin frequency of the lead compensator
α	upper cut-off frequency of lead compensator
τ	lower cut-off frequency of lead compensator
T_{s}	sampling period

1 Introduction

The use of renewable energy sources, where DC power is converted into AC power, and the widespread use of voltage sensitive electronic devices have triggered the market and researchers to develop new inverter technologies [1–3]. High-quality output power and efficiency are commonly issued objects in grid connected and stand-alone mode power conversion applications. One of the most widely used inverter models in stand-alone mode operation is the voltage source inverter (VSI) model, in which the output voltage of the inverter should be controlled to guarantee nominal voltage for all types of loads [4, 5].

In VSIs, the multi-level topologies, especially three-level (3L), are currently more preferred than 2L topologies since they offer lower total harmonic distortion (THD) and higher efficiency. Among the 3L inverters, neutral point-clamped (NPC)-based topology is one of the most well-known topologies and is preferred in many industrial power electronic applications [6, 7]. Nowadays, the T-type NPC (T-NPC) topology has been used as it provides higher efficiency and simple operation principle requirements [8]. Along with the developments in semiconductor technologies, new topologies can be derived from the change of the switching element employed in the topology. With the improving of insulated gate bipolar transistor (IGBT) technology, the newly developed advanced T-NPC (AT-NPC) topology is becoming prominent in low-voltage applications. Thanks to the reverse blocking IGBT (RB-IGBT), this topology provides higher efficiency and larger reverse blocking voltage capacity [9]. In our recent study [10], we investigated the performance of the on-grid AT-NPC inverter comparing with T-NPC topology. In [11], the three-phase AT-NPC

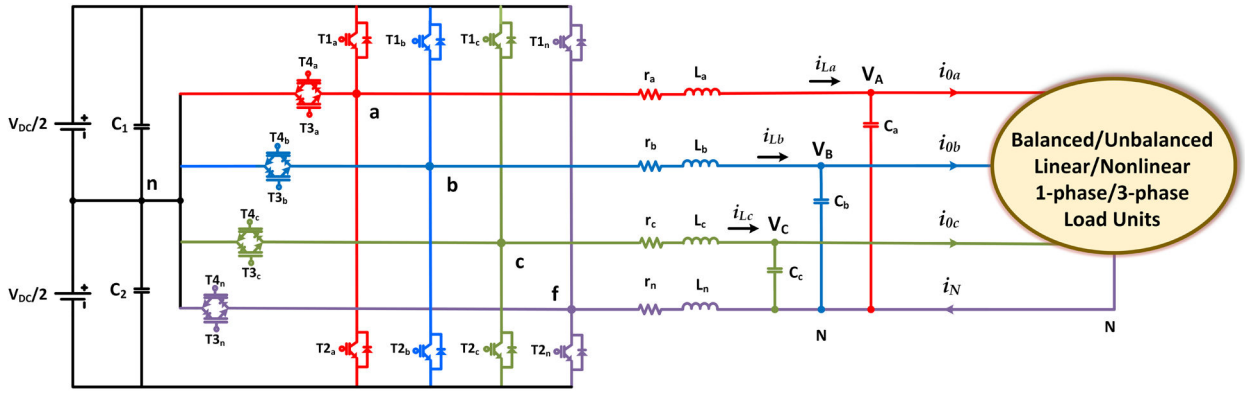

Fig. 1 *Structure of the proposed 3L 3P4L AT-NPC inverter system*

inverter is employed in an induction motor application. While the structure of the 3L three-phase four-leg (3P4L) stand-alone mode AT-NPC inverter is firstly investigated in this work.

In three-phase systems, maintaining nominal balanced sinusoidal voltage to the load connected at the inverter output terminals is not always possible especially in the presence of unbalanced or non-linear load conditions. These types of loads require additional paths for zero sequence voltage and current. In order to provide nominal balanced voltages, three-phase four-wire (3P4W) systems present the fourth current path for zero sequences between the load and split DC-link capacitor. In this case, large DC-link capacitors are needed to handle zero voltages, otherwise, there will be differences in the inverter output voltage levels. The usage of a delta/zigzag or delta/star connected transformer at the load side can be considered as another solution, however, the used transformer makes the system disadvantageous [12].

Apart from the 3P4W system, the 3P4L structure, which is widely used in active filtering, uninterruptable power supply systems, standalone mode renewable energy conversion systems, dynamic voltage restorers, and many military, medical, and telecommunication applications can provide all types of loads with nominal balanced voltages [13]. In this structure, an additional fourth leg in the inverter creates a path for neutral current. However, with the additional fourth leg, the complexity and controller design procedure of the topology is increased to obtain high-quality output voltage and high performance under all types of loads. In the literature, many linear control techniques such as the proportional–integral (PI) controller can be adopted to the 3P4L inverter topology. Owing to the inherit characteristic, the PI control cannot track a sinusoidal reference signal without a steady-state error. Therefore, it needs additional coordinate transformation such as *abc* to *dq*0 coordinates and needs an inverse coordinate transformation for pulse width modulation (PWM) signals generation. Moreover, a distinct controller must be designed for zero sequence voltage [14–20]. These all increase the computational burden of the microcontroller and complexity of the PI controller design. On the other hand, modern control techniques such as predictive and deadbeat controller for the 3P4L inverter can be found in [13, 21, 22]. Additionally, as being a non-linear control technique, a sliding mode controller is presented in [23, 24] for four leg inverters. Although these modern and non-linear control techniques provide high performance and wide range stability regions, they usually suffer from the complexity and inaccuracy of the system model [16]. As an alternative controller, the proportional multi-resonant (PMR)-based controller has been proposed by different researchers. The fundamentals of the PMR controller can be found in [25, 26]. In [27], the PMR-based double-loop controller design is widely investigated for a single-phase inverter. However, in the inner loop of the controller, the capacitor's current feedback is used for an active damping method, which requires an expensive current sensor and is not able to protect the inverter against over-current problems. In [28], the PMR controller is designed for a three-phase three-leg inverter with an inverter current sampled double-loop controller. In the other work [29], the PMR controller is employed for only two-level 3P4L conventional H-bridge topology. A recent study [30] presents a PMR controller for a power ground unit with an NPC type inverter. However, this structure has less efficiency as compared to recently proposed AT-NPC topology [10, 11]. Moreover, the complexity of the system is increased with the employed 3D space vector modulation (SVM).

In this study, a 3L 3P4L AT-NPC inverter system is proposed to feed nominal balanced voltage to all types of loads with a double-loop controller. The use of the PMR controller to compensate certain low-order harmonics in the outer voltage loop offers a simple controller design and reduced computational burden for the 3L 3P4L AT-NPC inverter system because it does not include any axes transformation and non-linear controller. For the inner loop, although an employed inverter current sampled inner loop limits the phase margin (PM) of the system, it is used in order to provide high dynamic and steady-state performance and also over current protection. To achieve this, a lead compensator is also designed, which increases system PM over the stability limits. In the PWM generation stage, thanks to the independent controllability of each output voltage offered by the PMR controller, a simple carrier-based PWM (CBPWM) technique, unlike a space vector technique requiring more microcontroller sources, is used for a three-level (3L) four-leg inverter. With all these aspects, a simple and high-performance controller, which has not been presented in the literature, is achieved for the 3L 3P4L AT-NPC inverter system.

This paper organised as follows; in Section 2, the modelling of the proposed system is created for controller design. In Sections 3 and 4, step by step analytical controller design is given. In Sections 5 and 6, simulation and experimental results are given to validate effectiveness of the proposed system. The conclusion of the proposed system is given in the final section.

2 System structure and modelling

We consider a 3L 3P4L AT-NPC inverter, which consists of DC-link power source, RB-IGBT, conventional IGBT, inductor–capacitor-type filter, and load unit as shown in Fig. 1. The DC-link power stage is modelled with a voltage source and two DC capacitors to obtain three-level inverter output voltage (v_{inv}). Throughout this paper, the DC voltage of each capacitor is assumed to be balanced and constant. Each output phase of the inverter is connected to the load unit via filter inductor ($L_a = L_b = L_c = L$) and filter capacitor ($C_a = C_b = C_c = C$). Since equivalent series resistances (r_a, r_b, r_c) of the filter inductors provide damping to the system, these resistances are omitted in the controller design procedure to handle the worst condition. The inverter voltages after filtering supply the load unit with the output voltage ($V_A = V_B = V_C = V_{\text{out}}$).

Using Kirchhoff voltage and current laws, (1) and (2) can be easily written from Fig. 1 in *s*-domain with the assumption that the load current I_0 is a disturbance in the system

$$V_{\text{inv}}(s) = sLI_{\text{L}}(s) + \frac{1}{2}sCI_{\text{L}}(s) \tag{1}$$

$$V_{\text{out}}(s) = \frac{1}{sC} I_{\text{L}}(s) \tag{2}$$

Using these equations, the one-phase equivalent model of the inverter is formed as in Fig. 2.

3 Control structure of 3L 3P4L AT-NPC inverter

Many control techniques have been developed for the three-level three-phase inverter; however, most of them, for instance, a synchronous reference frame-based controller, cannot be directly applied to four-leg inverter systems because such inverter structures need to control each phase voltage independently. In order to solve this issue, four-leg inverter topologies are used in industrial applications. In this work, we introduce a four-leg AT-NPC inverter topology to effectively control the phase voltages independently. The proposed control structure is based on the PMR controller for the 3L 3P4L AT-NPC inverter by using a double loop control structure. In the controller design, the inner loop is formed with inductor current feedback and the outer loop is formed with capacitor voltage feedback as shown in Fig. 3. As can be seen from the figure, the voltage controller of each phase is independent of each other and the PWM signals of the fourth leg are generated by the CBPWM technique. In this technique, the offset voltage (v_{fn}) provides extra degree of freedom to the system and its value is calculated according to (3), where $v^*_{\min}$ is equal to the minimum of the phase reference voltages ($\min(v^*_{af}, v^*_{bf}, v^*_{cf})$) and $v^*_{\max}$ is equal to maximum value of the phase reference voltages ($\max(v^*_{af}, v^*_{bf}, v^*_{cf})$). The calculated offset voltage is added to phase reference voltages ($v^*_{af}, v^*_{bf}, v^*_{cf}$) to obtain modulation signals, which are compared with triangular carrier waves that produce three-level PWM signals for each leg, as in Fig. 4

$$V_{fn} = \begin{cases} -\dfrac{V^*_{\min}}{2}, & v^*_{\max} < 0 \\ -\dfrac{V^*_{\max}}{2}, & v^*_{\min} > 0 \\ -\dfrac{V^*_{\min} + V^*_{\max}}{2}, & \text{elsewhere} \end{cases} \tag{3}$$

4 Controller design

In the controller design procedure, firstly, an inner inductor current loop controller will be designed with the one-phase equivalent of the inner loop model. In the design of this loop, the filter resonance problem and the inner loop bandwidth are taking into account. Also, the cross-over frequency of the system is also taken into consideration, because this gain shifts the cross-over frequency of the whole controller, not just the inner loop.

After designing the inner loop controller, the PMR-based outer voltage loop will be considered. In this loop, the proportional part of the controller will be tuned firstly. Then integrator parts of the controller are designed according to each voltage harmonic at the inverter output.

With the designed inner and outer loop, the delay effect of the digital implementation will be included in system performance and stability analysis. Finally, a lead compensator design will be employed to compensate for the effect of the delay.

4.1 Inner inductor current loop controller design

The one-phase equivalent inner loop model of the system with inductor current feedback is given Fig. 5. In this loop, only proportional current controller (K_{CC}) is employed, although controllers with an integral term such as PI or proportional–resonant (PR) could be used. By doing so, the analysis and design of the controller are simplified. On the other hand, the high proportional gain is required to reduce the steady-state error. For this reason, a voltage reference feed forward path is employed in the controller design as in Fig. 3. By using (1) and (2), the closed loop transfer function of the inner current loop ($G_{\text{CC}}(s)$) can be

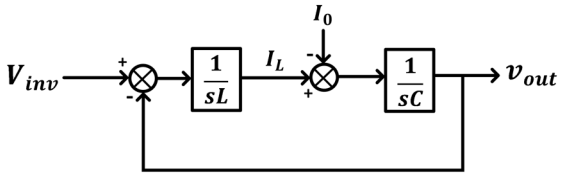

Fig. 2 *One phase equivalent model of the inverter*

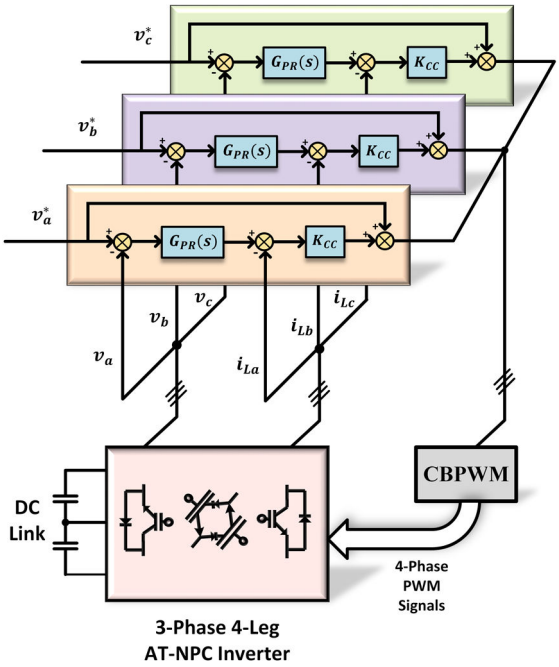

Fig. 3 *Suggested double loop controller block diagram for 3L 3P4L AT-NPC inverter system*

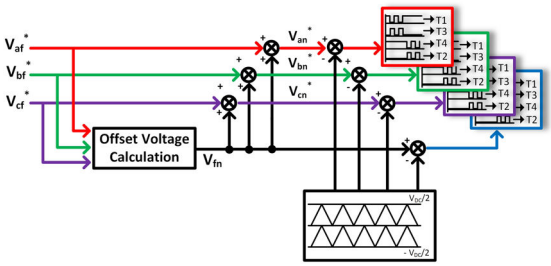

Fig. 4 *CBPWM technique for the 3L 3P4L AT-NPC inverter*

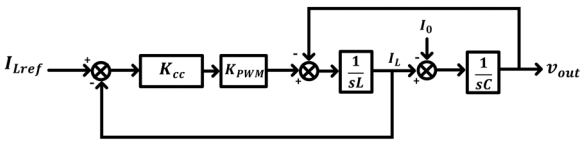

Fig. 5 *One-phase equivalent inner inverter current loop model of the system*

obtained as in (4) in accordance with Fig. 5, where K_{PWM} is the PWM gain, L and C are the filter inductor and capacitor, respectively

$$G_{\text{CC}}(s) = \frac{(I_{\text{L}}(s))}{(I_{\text{Lref}}(s))} = \frac{(K_{\text{PWM}}K_{\text{CC}}Cs)}{(CLs^2 + K_{\text{PWM}}K_{\text{CC}}Cs + 1)} \tag{4}$$

It is clearly shown from (4) that the closed loop gain of the inner loop depends on the product of K_{PWM} and K_{CC} (with the assumption that the filter capacitor is predetermined). Therefore, the design of the proportional gain $K_{\text{PWM}}K_{\text{CC}}$ is an important parameter for the system dynamic and steady-state performance. Furthermore, the inner loop also provides active damping of the filter resonance to the system. This damping effect can be shown in

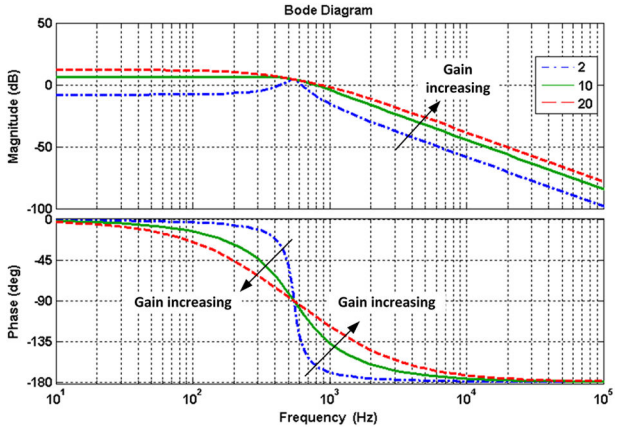

Fig. 6 *Bode plots of the open loop system ($v_{out}(s)/v_{ref}(s)$) for different inner loop proportional gains ($K_{PWM}K_{CC} = 2, 10, 20$) considering only a constant outer proportional loop gain K_{VC}*

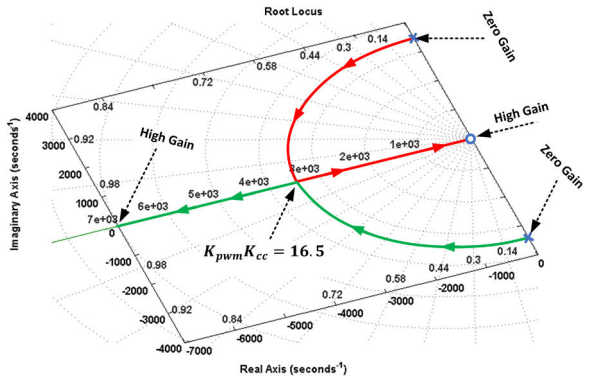

Fig. 7 *Root locus diagram of the inner inverter current loop*

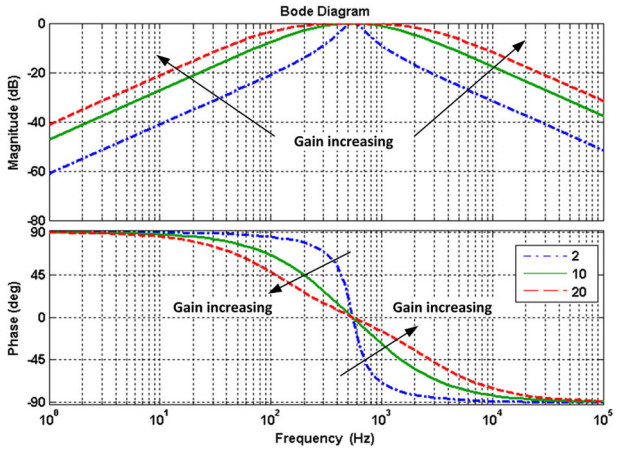

Fig. 8 *Bode plots of the closed loop system ($v_{out}(s)/v_{ref}(s)$) with only a constant outer proportional loop gain for different inner loop proportional gains ($K_{PWM}K_{CC} = 2, 10, 20$)*

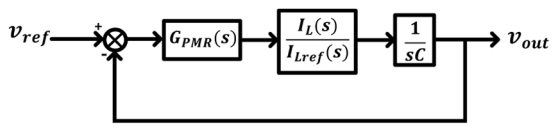

Fig. 9 *PMR based outer loop one-phase model for the proposed system*

Fig. 6 where the open loop bode plot of the system with a random outer proportional controller loop (outer loop controller will be designed in the following section) is given for different $K_{PWM}K_{CC}$ values.

As can be seen, this gain affects the whole controller frequency response, not just the inner loop. One can also observe from the figure that the cross-over frequency (f_c) of the system shifts with different $K_{PWM}K_{CC}$ gain values. Increasing this gain reduces the resonance effect and also increases cross-over frequency of the whole system.

Additionally, as can be seen in Fig. 7 which shows the root locus diagram of the inner loop, this $K_{PWM}K_{CC}$ gain moves the roots of the inner loop towards the over lapped position by increasing from zero to 16.5 values. In the way of the increasing of the gain, the damping coefficient ζ reaches the maximum value of 1. Increasing the gain after the value of 16.5 can be considered. However, the upper limit of the gain is limited by the inner loop bandwidth up to switching frequency (f_{sw}). As Fig. 8 illustrates, by increasing $K_{PWM}K_{CC}$, the internal loop bandwidth also increases. In practice, the bandwidth is selected enough lower than the switching frequency to reduce the switching noise in the inner loop. In the desired bandwidth frequency (w_{bw}), the magnitude of $G_{CC}(s)$ is equal to $1/\sqrt{2}$ ($|G_{CC}(s)| = 1/\sqrt{2}$). With this equation, the upper limit of the $K_{PWM}K_{CC}$ gain can be checked according to (5). In this work, the $K_{PWM}K_{CC}$ gain is determined as 16.5, which is smaller than $w_{bw} = f_{sw}/2$ bandwidth that guarantees system stability and provides higher controller performance

$$K_{PWM}K_{CC} = \frac{CL\omega_{bw}^2 - 1}{C\omega_{bw}} \tag{5}$$

4.2 Outer capacitor voltage loop controller design

Once the inner loop controller is designed for the proposed 3L 3P4L inverter system, then a PMR-based outer loop controller can be designed to control the output voltage of the inverter. As the proposed inverter supplies voltage to linear unbalanced or non-linear load types, the zero sequence voltages, and low order harmonics should be controlled. To achieve these functionalities in the proposed system, the output voltages of each phase should be controlled independently. Therefore, in the output voltage control, unlike a PI controller, a PMR-based controller is employed in the outer loop which does not require any axis transformation and reduces the computational burden of the microcontroller. In Fig. 9, the PMR controller-based outer voltage loop is given for one phase of the proposed system.

In (6), the transfer function of the PR controller ($G_{PR}(s)$) is given. In this equation K_{VC}, K_{i1}, w_{c1}, and w_1 represent the proportional part of the PR controller, integrator gain for fundamental frequency, cut-off frequency, and fundamental frequency, respectively. As expected, $G_{PR}(s)$ provides high gain at only fundamental frequency; however, (6) can be expanded for unwanted multi low-order harmonics (h) as in (7) where K_{VC} represents the proportional part of the PMR controller and h indicates the harmonic order in which frequency determines PMR controller resonant frequency (w_h). Therefore, using a PMR controller, each harmonic in the content of the output voltage can be individually and effectively suppressed and zero steady-state error can be achieved

$$G_{PR}(s) = K_{VC} + \frac{K_{i1}\omega_{c1}s}{s^2 + 2\omega_{c1}s + \omega_1^2} \tag{6}$$

$$G_{PMR}(s) = K_{VC} + \sum_{h\,=\,1,3,5,7,9} \frac{K_{ih}\omega_{ch}s}{s^2 + 2\omega_{ch}s + \omega_h^2} \tag{7}$$

In the controller design, the dynamic performance of the fundamental frequency is mainly determined by the proportional part of the PMR controller (K_{VC}). Also, this proportional part affects system stability. Hence, a well-designed proportional gain in the PMR controller would give a better transient response and enhance the stability of the system. To evaluate the K_{VC} effect on the closed loop system in (8), the integrator part of each harmonic compensator (HC) can be taken as zero ($G_{PMR}(s) = K_{VC}$), since the integrator part of each HC have almost no effect on system phase and gain margin. As can be seen in Fig. 10, all of the investigated cases have the same phase plot, therefore, the decreasing of K_{VC}

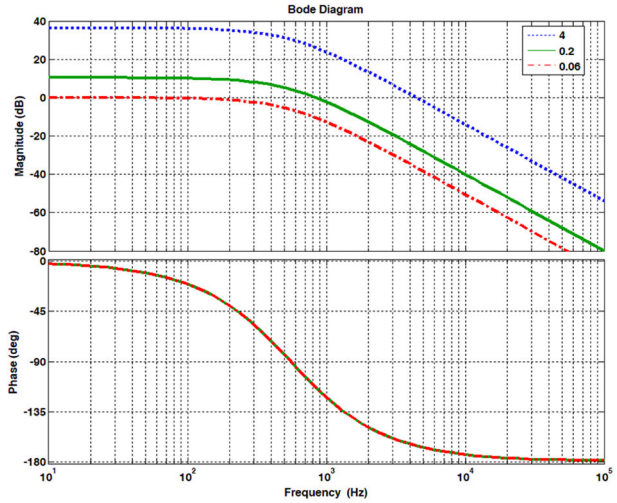

Fig. 10 *Bode plots of the closed-loop system ($v_{out}(s)/v_{ref}(s)$) with the condition of $G_{PMR}(s) = K_{VC}$ for $K_{VC} = 4, 0.2, 0.06$ values*

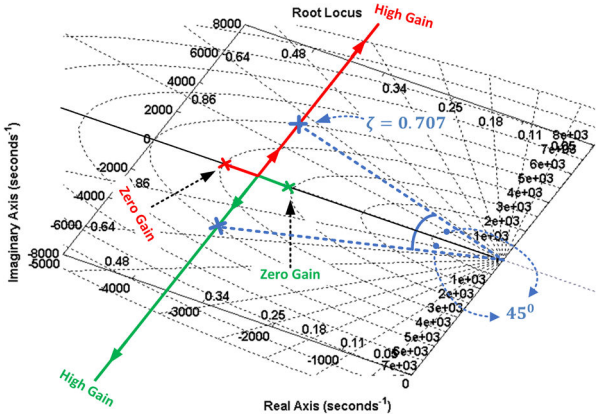

Fig. 11 *Root locus diagram of the system ($v_{out}(s)/v_{ref}(s)$) with $G_{PMR}(s) = K_{VC}$ condition*

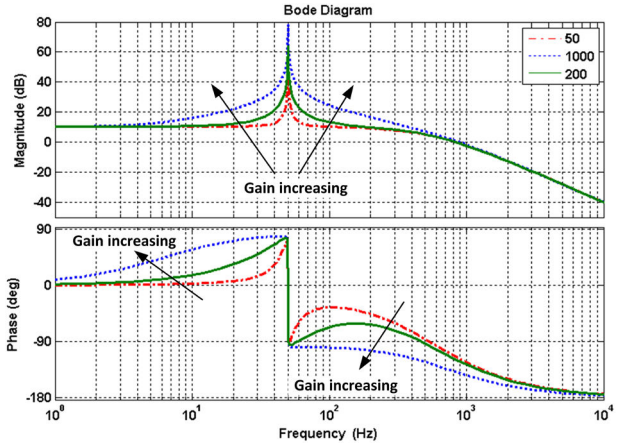

Fig. 12 *Bode plots of the system ($v_{out}(s)/v_{ref}(s)$) with the conditions of $G_{PMR}(s) = K_{VC}$ and K_{VC} is constant for different K_{ih} values*

causes a decreasing of the cross-over frequency (f_{co}), which leads to a higher PM of the system. On the other hand, improved system transient response can also be achieved by increasing K_{VC}. As a result, there is a trade-off between system transient response and stability in the determination of K_{VC}. In order to obtain optimum performance, the loop gain $K_{VC} = 0.06$ can be chosen where the angle of the roots with real axis is 45° that offers $\zeta = 0.707$ as shown in Fig. 11. However, this proportional value is not large enough to locate magnitude curve of the system over 0 dB (see Fig. 10) which would make system unstable. Therefore, a larger $K_{VC} = 0.2$ is selected to put up magnitude curve of the system with minimum performance loose

$$\frac{v_{out}(s)}{v_{in}(s)} = \frac{G_{PMR}(s)G_{CC}(s)}{sC + G_{PR}(s)G_{CC}(s)} \tag{8}$$

After selecting the proportional part of the PMR controller ($G_{PMR}(s)$), the integrator gains of each HC (K_{ih}) can be tuned to suppress the voltage harmonic caused by the load current. These integrators have effects only in the vicinity of their resonant frequency (w_h) with the condition that the cross-over frequency of the system must be higher than resonant frequency of each HC ($2\pi f_c > \omega_h$). As can be seen in Fig. 12, these gains (with a constant K_{VC} and K_{CC}) determine only the resonance peak amplitude and bandwidth around the resonance frequency. By increasing these, the steady-state and phase error of corresponding harmonics (h) can be reduced. However, the system stability also should be taken into account for complete analysis to determine the upper limit of these gains (K_{ih}). Hence the transfer function of the PMR controller can be reduced for each HC individually ($h = 1, 3, 5, 7$) and the yield of each $G_{PMR}(s)$ transfer function is substituted in (8). This yields a closed loop transfer function for each HC separately as given in (9) where the denominator can be used to determine the stability limit of the system for each proportional part of the integrator (K_{ih}) by applying Routh–Hurwitz criteria. The stability limit of the system for each HC integrator gain (K_{ih}) derived as in (10) as a result of the Routh–Hurwitz criteria. By using criteria stated in (10), the upper limit of the integrator gains (K_{ih}) of each HC for the stable system can be found. In this way, the upper limit of the integrator gains of each HC can be derived as 3643, 1165, 699, 499, and 388 for first, third, fifth, seventh, and ninth HC, respectively. However, in our work, the implemented values are chosen to be smaller than the limit values to suppress corresponding voltage harmonics resulting from severe load type. In this way, the system would be stable in case of a possible parameter uncertainty while the steady-state and phase error of the designed controller converges to zero.

(see (9))

(see (10))

4.3 Delay effect and lead compensator design

In previous sections, all the parameters of the PMR and inner loop controller are tuned. However, the phase and gain margin of the whole system must be evaluated to guarantee system stability. In Fig. 13, open loop frequency response of the designed system is given. We can see that the designed system has enough phase and gain margin to be stable. Nevertheless, a digital implementation of the proposed system affects its margins since it introduces the inherent time delay, which decreases controller performance and stability limits. This delay effect practically is composed of the following: the PWM update delay time (T_{PWM}), digital sampling delay time (T_{samp}) and the computation delay time (T_{comp}). The sum of these delay times represents total delay time T_d as expressed in (11). The total time delay T_d can be described in the s-domain as $e^{-T_d s}$, which has no effect on the system magnitude. In practice, this time delay is usually considered as one or two sampling period (T_s) time and it depends on the PWM and sampling methods [31, 32]. In this work, the double update PWM method is used. Also, the sampling instants are shifted to the

$$\frac{v(s)}{v^*(s)} = \frac{s^3(K_{CC}K_{VC}K_{PWM}) + s^2(K_{CC}K_{PWM}(K_{ih}\omega_{ch} + 2K_{VC}\omega_{ch})) + s(K_{CC}K_{VC}K_{PWM}\omega_h^2)}{s^5(LC) + s^4(CK_{CC}K_{PWM} + 2LCw_h) + s^3(CL\omega_h^2 + K_{CC}K_{VC}K_{PWM} + 2CK_{CC}K_{PWM}\omega_{ch} + 1)} \tag{9}$$
$$+s^2(CK_{PWM}K_{CC}w_h^2 + 2w_{ch} + K_{CC}K_{PWM}K_{ih}w_{ch}^2 + 2K_{CC}K_{VC}K_{PWM}w_{ch}) + s(w_h^2 + K_{CC}K_{VC}K_{PWM}\omega_h^2)$$

$$K_{ih} > \frac{(CK_{CC}K_{PWM} + 2LCK_{PWM})(CL\omega_{h^2} + K_{CC}K_{PWM}K_{VC} + 2CK_{CC}K_{PWM}\omega_{ch} + 1) - CL(CK_{CC}K_{PWM}\omega_{h^2} + 2\omega_{ch} + 2K_{CC}K_{PWM}K_{VC}\omega_{ch})}{CLK_{CC}K_{PWM}\omega_{ch}} \quad (10)$$

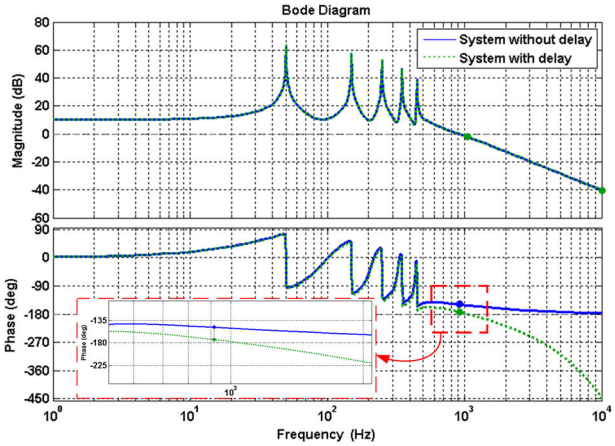

Fig. 13 *Bode plots of the system with and without delay effect with time delay* $T_d = 1.5T_s$

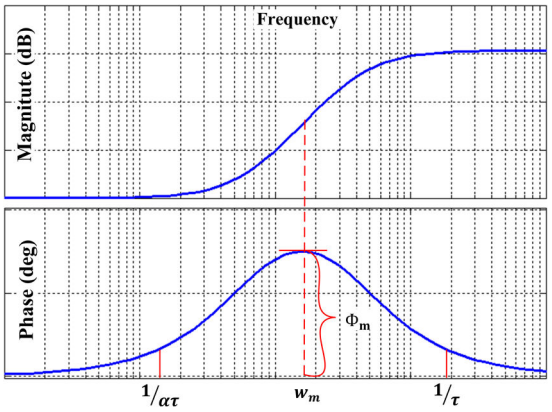

Fig. 14 *Bode plot of a traditional lead compensator*

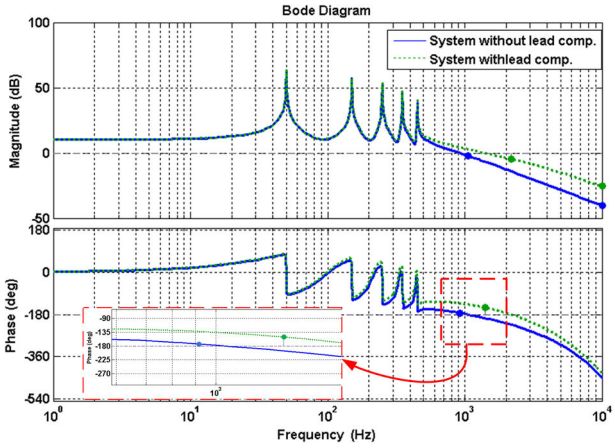

Fig. 15 *Bode plots of the system (including delay time effect) with and without designed lead compensator*

middle of the PWM signal to reduce harmonic disturbances. Therefore, the total time delay T_d is considered as $1.5T_s$ time. In Fig. 13, the open loop frequency response of the system with time delay $T_d = 1.5T_s$ is shown where we can observe that the PM value of the system is reduced enough to make it unstable

$$T_d = T_{PWM} + T_{samp} + T_{comp} \quad (11)$$

Table 1 System parameters

Parameter	Value (unit)
output voltage (line to neutral)	110 V_{rms}
output frequency	50 Hz
phase filter inductor	2.4 mH
neutral leg inductor	0.5 mH
phase filter capacitor	35μF
DC bus voltage	450 V
DC capacitors	2200μF
switching frequency	20 kHz
sampling frequency	20 kHz

To improve the system PM for stability, a lead compensator given in (12) is employed in the outer voltage control loop. In the lead compensator design procedure, the parameter maximum PM that can be added to the system (Φ_{max}) and its located frequency (w_m) are first to be determined. Following (13) and (14) and with the help of Fig. 14, the appropriate α (upper cut-off frequency) and τ (lower cut-off frequency) values can be obtained. In the traditional lead compensator design problem, the value of w_m and Φ_{max} can be determined according to the crossover frequency of the system and the required PM. However, in this way, the addition of a lead compensator in which the angle Φ_{max} is selected as the system's crossover frequency ($w_m = 2\pi f_c$) deviates the magnitude curve of the system from the original one as shown in Fig. 15. This is due to the fact that the lead compensator has a magnitude different from 1 dB at the w_m frequency. Therefore, in this work, w_m is selected as 10 krad/s, which is larger than the crossover frequency. Since this could cause the degrading effect of HCs on the system's PM, a higher Φ_{max} value of 45° is selected. With these settings, the frequency response of the system with the designed lead compensator can be seen in Fig. 15. We can see clearly from this figure that the increased PM of the system is large enough to make it stable

$$G_{lead}(s) = \frac{\alpha\tau s + 1}{\tau s + 1} \quad (12)$$

$$\Phi_m ax = \sin^{-1}\left(\frac{\alpha - 1}{\alpha + 1}\right) \quad (13)$$

$$\omega_m = \frac{1}{\tau\sqrt{\alpha}} \quad (14)$$

5 Simulation studies

The proposed system is first built in PSIM simulation software with the listed parameter in Table 1 to verify the theoretical analysis given in pervious sections. Then the experimental studies are conducted where the proposed 3L 3P4L AT-NPC system's power stage is modelled with RB-IGBTs using the thermal module of PSIM. With the calculated PMR controller parameters, the steady-state performance of the proposed inverter system is tested under a highly non-linear load unit and an unbalanced load unit. In addition, the dynamic performance of the system with the step load change is also tested for further examination.

A non-linear type load, given in Fig. 16, is connected to each phase of the proposed inverter output. Under this load type, the phase currents, neutral current and output voltages of the inverter are given in Fig. 17. The THD value of the output voltage in the figure is about 2.4% for each phase voltage under the highly non-linear load. This result shows that the proposed structure has effective performance and does not cause large disturbances in the output voltages.

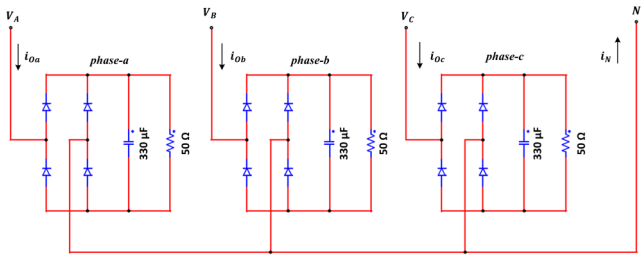

Fig. 16 *Non-linear load created with single-phase diode rectifier bridge*

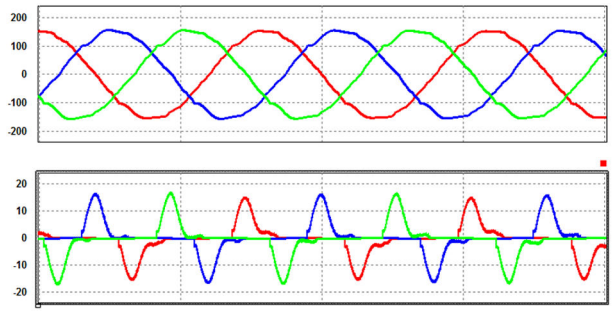

Fig. 17 *Simulation result of the system under a highly non-linear load type. Upper waves are output phase voltages and the lowers are load currents*

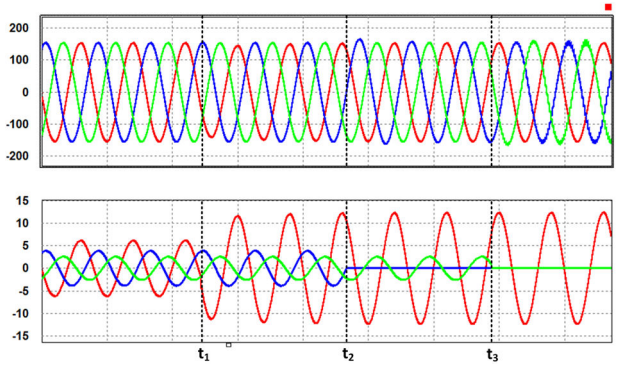

Fig. 18 *Simulation result of the system under a linear dynamic load type. Upper waves are output phase voltages and the lowers are load currents*

In order to investigate the dynamic performance and independent controllability of each phase voltage, the simulations are carried out and the results are given in Fig. 18. As can be seen, the proposed inverter system starts with an unbalanced 25, 50 and 60 Ω load and then at the time instant t_1, the load of the phase-a is increased to the nominal load from half of it. In the time intervals $[t_2 - t_3]$ and $[t_3 - \text{inf}]$, the loads phase-b and phase-c are disconnected from the system, respectively. In this situation, the system can keep supplying nominal voltage to the connected two-phase and one-phase loads.

In the application of an inverter, the filter parameters have an essential role in system stability and performance. The value of L and C, in practice, may deviate from the exact values with the operation condition or attrition. Therefore, the robustness performance of the designed control system should be evaluated to take into account the deviations in the system parameters. Fig. 19 shows the PM and output voltage THD of the designed system for different filter L and C parameters. As shown in Fig. 19*a*, the designed closed loop control system has sufficient PM to be stable in the wide range of the filter parameters deviation. The output voltage THD with respect to the filter parameter deviations is given in Fig. 19*b*. These clearly show the robustness of the designed system. On the other hand, the decrease in the deviation of the filter parameters, L and C, may cause an increase in the output THD since the filter resonance is suppressed by active damping method. To handle this problem, the inner loop controller gain

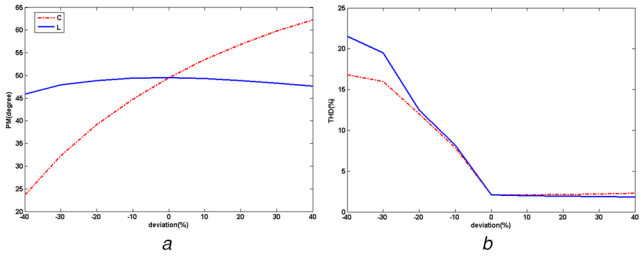

Fig. 19 *Designed system*
(a) PM, ***(b)*** Output voltage THD value under deviating filter parameters

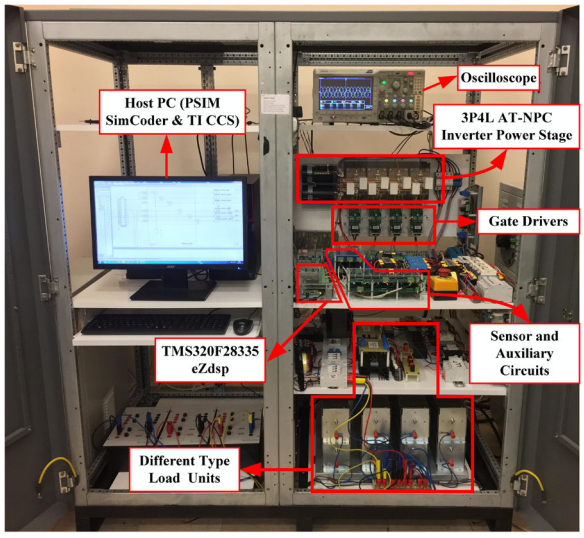

Fig. 20 *Experimental setup of the 3L 3P4L AT-NPC inverter system*

should be updated in accordance with the controller design procedures as stated in the previous sections.

6 Experimental validation

To evaluate effectiveness of the proposed control system, the 3L 3P4L 2.5 kVA AT-NPC inverter system, as shown in Fig. 20, has been established with a DC voltage source, 4MBI300VG-120R-50 RB-IGBT modules from Fuji Electronic, LC filter, gate drivers, various load types, signal conditioner circuits, protection, and sensor circuits. The proposed control algorithm is implemented with a 32-bit floating point TMS320F28335 eZdsp Kit from Texas Instrument. In all measurements and HD analyses, the Tektronix MDO3024 200 MHz oscilloscope and the MDO3PWR power analyser module are used. In the experimental study, the parameters of the system and controller are the same as stated in previous sections.

In the first step of an experimental study, the steady state and dynamic performance of the proposed system are investigated with unbalanced resistance and resistance–inductance type load, which can be modelled as space heaters and electrical machines, respectively. In Fig. 21, the inverter output voltages and neutral current are shown in steady-state. As can be seen, the neutral current of the system is different from zero because of the unbalanced condition. The figure also shows that the output voltages of the system can track balanced nominal reference voltages with excellent steady-state error of 1.2% rms voltage (average of three phases) and with lower than 2% THD under unbalanced linear load types. Fig. 22 shows the inverter system response to the positive 50% step load change from half of the nominal load to the nominal under resistive unbalanced load condition of which parameters can be seen in Table 2. Owing to the high dynamic performance of the designed controller, during the transition state the volt-second lost in the output voltages, defined in [16], is very low. Furthermore, the step load change in a phase does not affect the other phase voltages thanks to the designed controller ability of independent control of each phase. These

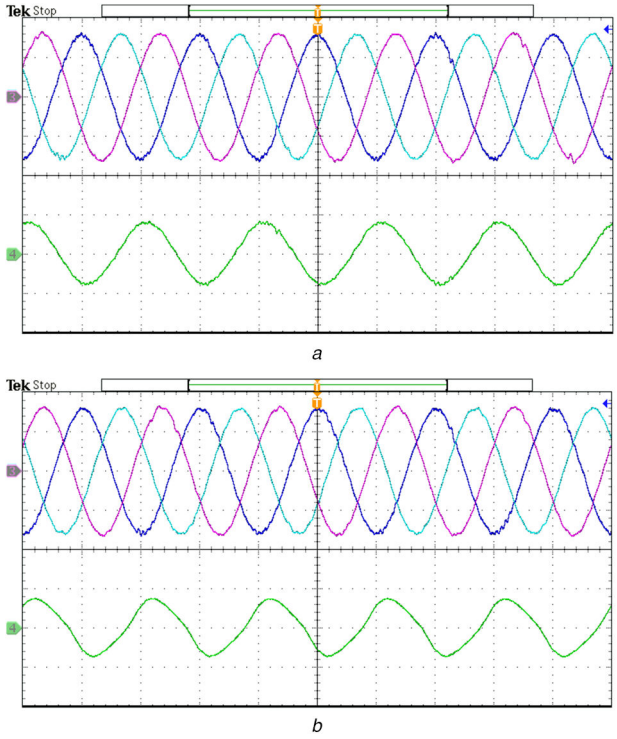

Fig. 21 *Experimental results of the system under unbalanced linear*
(a) Resistive and ***(b)*** Resistive-inductive load type. Ch1, Ch2 and Ch3 are output voltage (100 V/div). Ch4 is a load current (10 A/div)

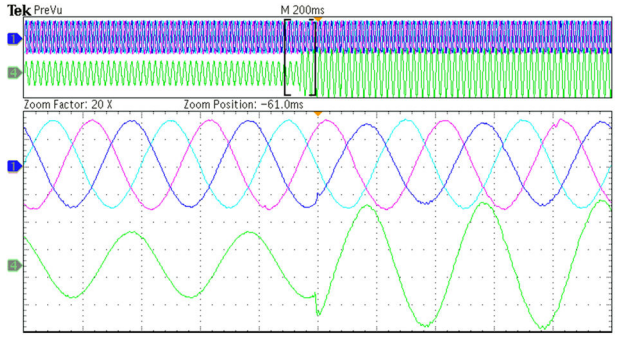

Fig. 22 *Experimental results of dynamic performance evaluation of the system with a 50% step load change. Ch1, Ch2 and Ch3 are output voltage (100 V/div). Ch4 is a load current (10 A/div)*

confirm prospering dynamic performance of the designed controller.

The steady-state performance of the proposed 3P4L AT-NPC inverter system in the case of non-linear load feeding is tested with a single and three-phase diode rectifier bridge followed by a capacitor depicted in Figs. 16 and 23. These types of loads are used for modelling non-linear loads employed in industrial and domestic applications such as motor drivers, PC power supplies, and electronic ballasts. Also, it is defined as the most severe non-linear load by international standards such as IEC 62040-3. Under this type of load, a phase current, seen in Fig. 24, has 37.5% THD that forces the output voltage shape to deviate sinusoidal wave form. As shown in Fig. 24, the proposed system in this experiment presents a small THD of 2.24% (average of three phases) at the output voltages.

To further investigate the performance of the proposed structure, we test the system under a highly non-linear load type as depicted in Fig. 16. Owing to the absence of any inductor between the load and the inverter output, the load currents have sharp spike that causes 105% THD in the load currents and strongly forces the output voltages of the system to deviate sinusoidal wave form. Fig. 25 shows the output voltages and a phase current under this serious non-linear load. Although the fourth leg current frequency is three times the load current (150 Hz) arising from the load

Table 2 Summary of the experimental results

Load type	Each phase load values	Output voltages (error)	Output currents (rms)	Output voltage THD (%)
linear resistive unbalanced	12.5 Ω	110 V (0%)	8.4 A	1.89
	25 Ω	111 V (0.9%)	4.3 A	1.87
	50 Ω	113 V (2.7%)	2.2 A	1.55
linear RL unbalanced	(series) 12.5 Ω and 16.5 mH	111 V (0.9%)	7.5 A	1.89
	(series) 25 Ω and 35.5 mH	111 V (0.9%)	3.8 A	1.89
	(series) 50 Ω and 57.5 mH	114 V (3.6%)	1.9 A	1.95
non-linear three-phase diode rectifier bridge	50 Ω and 470μF	112 V (1.8%)	4.03 A	2.21
		111 V (0.9%)	4.05 A	2.04
		114 V (3.6%)	4.01 A	2.49
highly non-linear	(parallel) 50 Ω and 330μF	111 V (0.9%)	5.10 A	2.89
one-phase diode	(parallel) 50 Ω and 330μF	112 V (1.8%)	5.10 A	2.87
rectifier bridge	(parallel) 50 Ω and 330μF	113 V (2.7%)	5.15 A	2.86

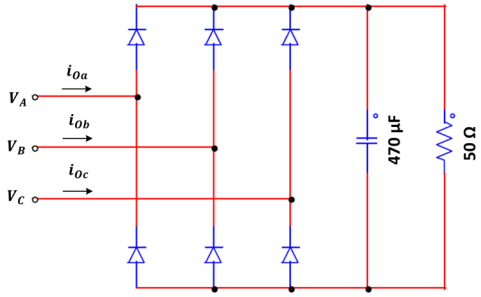

Fig. 23 *Non-linear load created with the three-phase diode rectifier bridge*

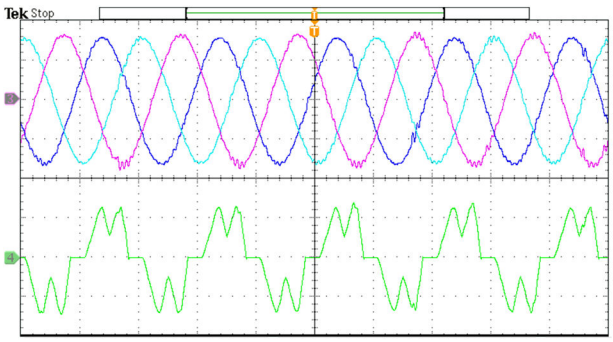

Fig. 24 *Experimental results of the system under three-phase diode rectifier bridge non-linear load. Ch1, Ch2 and Ch3 are output voltage (100 V/div). Ch4 is a load current (10 A/div)*

characteristic, the output voltage waveforms are well-compensated by the designed controller with low THD value <3%. This is evidence that the designed controller is robust even under seriously distorted load and can withstand different load types with small THD in the output voltages. All the detailed experimental results are also listed in Table 2.

The proposed inverter current sample-based double-loop PMR controlled system is compared with other works given in Table 3. Although the transient response performances of the non-linear control methods given in [13, 23] are better than the proposed method, the proposed PMR-based control method has features that lower complexity and computational burden. On the other hand, the linear method given in [28] can be expanded for a four-leg

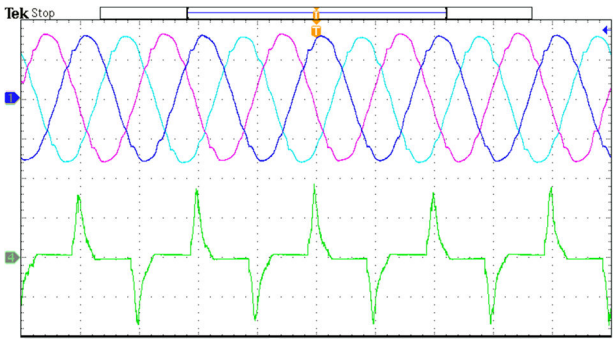

Fig. 25 *Experimental results of the system under serious non-linear load. Ch1, Ch2 and Ch3 are output voltage (100 V/div). Ch4 is a load current (10 A/div)*

Table 3 Comparison of the proposed system with other works

Reference	[13]	[23]	[28]	Proposed system
switching frequency	not fixed	10 kHz	20 kHz	20 kHz
robustness	high	very high	high	high
PWM method	3D-SVM	3D-SVM	—	CBPWM
linear load performance	very high	very high	very high	very high
non-linear load performance	high	high	high	very high
transient response performance	very high	very high	very high	high
inverter current sampling	yes	Yes	no	yes
complexity	high	very high	low	very low
computational burden	high	very high	low	low

inverter; however, it includes axes transformation that is not required for the proposed system thanks to independent control of each phase voltage. Additionally, Monfared *et al*. [28] have no inverter current sampling loop to protect the system against overcurrent problems in industrial applications. This comparison shows that the promising improvement and reduced complexity in the control of 3L 3P4L inverter output voltages are achieved by the proposed control method.

7 Conclusions

This study proposes an analytical PMR-based controller design for a 3L 3P4L AT-NPC inverter system to independently regulate instantaneous output voltages of each phase. Employing the sensed inverter current in the inner loop, the active damping of the filter resonance and the protection of the circuit are achieved, which also increases the system steady-state and dynamic performance. In the outer voltage loop, a PMR controller is designed to eliminate the effects of the load current low-order harmonics on the output voltage. Moreover, with the reference voltage feedforward path the output voltages of the inverter could be precisely regulated at the fundamental frequency. Since the controller is applied to each phase independently, there is no need to implement any coordinate transformation, which reduces the complexity and computational burden of the microcontroller. Although the using of an inverter current sampled double loop controller presents advantages, the PM of the system is inherently limited. To further increase the system PM, a lead compensator is also employed that guarantees the system stability in the wide range of parameters deviation and increases controller performance. To evaluate the performance of the proposed system, the experimental setup has been launched with balanced, unbalanced, and non-linear load types after the simulation studies. The results have confirmed the effectiveness of the proposed system both with steady-state and dynamic performances.

8 Acknowledgment

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