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A comparative study regarding effects of interfacial ferroelectric $Bi_4Ti_3O_{12}$ (BTO) layer on electrical characteristics of Au/*n*-Si structures

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Abstract. **Present study focuses on the effects of interfacial ferroelectric BTO layer on the electrical characteristics of Au/*n*-Si structures, hence Au/*n*-Si (MS) and Au/BTO/*n*-Si (MFS) structures were fabricated and admittance measurements (capacitance–voltage: *C–V* and conductance–voltage: *G*/*ω*–*V*) of both structures were conducted between 10 kHz and 1 MHz at room temperature. Results showed that *C–V* and *G*/*ω*–*V* characteristics were affected not only by frequency but also through deposition of BTO layer. Some effects can be listed as sharper peaks in *C–V* plots, higher capacitance and conductance values. Structure's series resistance (R_s) also decreased due to BTO layer. Interface states (N_{ss}) profiles of the structures were obtained using Hill–Coleman and high-low frequency capacitance (C_{HF}–C_{LF}). Some of the main electrical parameters were extracted from C^{-2}–*V* plots using depletion capacitance approach. Furthermore, current–voltage characteristics of MS and MFS structures were presented.**

Keywords. **Metal–ferroelectric–semiconductor (MFS) structures; $Bi_4Ti_3O_{12}$ (BTO); series resistance; interface states.**

1. Introduction

In the last few decades, ferroelectric materials have attracted great attention for non-volatile random access memory (NVRAM) applications. Having higher dielectric constant and lower coercive field have made these materials a suitable candidate as gate dielectric materials for various memory devices such as ferroelectric random access memories (FeRAMs), field effect transistors (FETs) and alike (Sugibuchi *et al* 1975; Bozgeyik *et al* 2010; Gautam *et al* 2010; Tang *et al* 2010). When the gate dielectric is a ferroelectric material in FET, the gate structure is basically a metal–ferroelectric–semiconductor (MFS) structure, hence these devices are also called as MFSFETs (Altındal *et al* 2008; Ren *et al* 2011). Consequently, performance of ferroelectric based memory devices is affected by MFS structure and its electrical characteristics. Therefore, over the past years, researchers have also focused on electrical characteristics of MFS structures (Kumar 2005; Wang and Ren 2005; Altındal *et al* 2008).

In the memory devices mentioned above, gate dielectric material is required to have low polarization fatigue, low coercive field, low leakage current, high remanent polarization and high permittivity for better results (Carrano *et al* 1991). Belonging to the Aurivillius family, bismuth titanate, $Bi_4Ti_3O_{12}$ (BTO), is a ferroelectric material which exhibits outstanding fatigue resistance when polarization switches with varying electrical field (Joshi and Krupanidhi 1993). BTO has a layered Aurivillius phase perovskite such that $(Bi_2Ti_3O_{10})^{-2}$ perovskite-like layers are sandwiched between $(Bi_2O_2)^{+2}$ sheets (Aurivillius 1949). BTO is indeed a promising ferroelectric material for various applications such as NVRAMs, optical displays, piezoelectric converters and sensors as a result of its unique properties of high dielectric strength, fast switching time, low polarization fatigue and coercive field, high refractive index, high Curie temperature of 950 K, etc. (Megriche *et al* 1999; Villegas *et al* 2004; Chia *et al* 2006; Parlaktürk *et al* 2008). Also, its perovskite layered form makes BTO suitable for lattice matched deposition on crystal substrates by various growth methods (Choopun *et al* 1995; Theis *et al* 1998), thereby making it suitable for various heterostructures including MFS structures.

C–V and *G*/*ω*–*V* measurement techniques are commonly used since, they allow quick determination of interface quality through extraction of electrical characteristics in various devices (Lappalainen *et al* 2004; Gökçen and Tunç 2013; Gökçen *et al* 2011; Nanda Kumar Reddy and Rajagopal Reddy 2012). Basically, this reveals the small-signal *C* and *G* data from which the main electrical parameters of these devices can be derived in the reverse bias region. Some of these parameters can be listed as doping concentration (N_D), built-in potential (V_{bi}), barrier height (Φ_B), R_s and N_{ss}. MFS structures basically behave like conventional MIS structures with a specific choice of ferroelectric material as insulator layer. In this respect, besides MIS structures, *C–V* and *G*/*ω*–*V* techniques can also be used for the characterization of MFS structures.

Although, there are studies which focused on BTO as ferroelectric material in MFS structures, most of these studies

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preferred *p*-Si as the semiconductor substrate. Due to rarity of studies concerning BTO/*n*-Si interface, *n*-Si was selected as semiconductor material in the present study. In our previous study (Gökçen and Yıldırım 2012), we investigated inhomogeneous barrier height of Au/$Bi_4Ti_3O_{12}$/*n*-Si structure with thicker BTO layer through Gaussian distribution of barrier height using current–voltage (*I–V*) measurements between 300 and 400 K. The aim of this study is to investigate the effects of BTO layer on the main electrical parameters of Au/*n*-Si structures by making comparisons between experimental data of the fabricated MS and MFS structures. Therefore, electrical characteristics of these structures were investigated using *C* and *G*/ω data obtained by admittance measurements between 10 kHz and 1 MHz as well as *I–V* measurements at room temperature.

2. Experimental

The studied structures were fabricated using *n*-type (*P*-doped) single crystal silicon wafer with ⟨110⟩ surface orientation, 280 μm thick, with 3″ diameter and 4·45 Ω·cm, resistivity. In the first step of cleaning, the wafer was ultrasonically cleaned by acetone, propanol and deionized water for 10 min at each step. Following the first step, the piranha solution ($3H_2SO_4$:$1H_2O_2$) was prepared for cleaning the organic residues. Then, the wafer was immersed into the solution for 15 min. In the last step, the wafer was dipped into the solution of 20% HF to get rid of the oxide layer formed in the previous step. After each cleaning step, the wafer was rinsed thoroughly in deionized water of 18 MΩ-cm resistivity. Immediately after the surface cleaning, high purity Au metal (99·999%) with thickness of 2500 Å was thermally evaporated from the tungsten filament onto the whole back surface of the wafer in liquid nitrogen-trapped vacuum system in the pressure of 1×10^{-6} Torr. In order to achieve a good ohmic contact, the evaporated Au was annealed at 700 K for 20 min. The front side of the wafer was cleaned with 20% HF solution to remove the thin oxide layer which was formed during annealing. Then, the wafer was cut into a few pieces. In order to form Au/$Bi_4Ti_3O_{12}$/*n*-Si structure, $Bi_4Ti_3O_{12}$ film was prepared onto the front side of Si wafer by the use of a magnetron sputtering having a hot compacting of $Bi_4Ti_3O_{12}$ powder of a stochiometric composition as a target material. The mixture of Ar and O_2 was used as a working medium and the substrate was kept at 700 K. The thickness of the deposited BTO thin films were found to be around 160 Å measured by Veeco Dektak 6 M thickness profilometer. After $Bi_4Ti_3O_{12}$ film was deposited onto Si wafer, circular dots of 2 mm in diameter and 2500 Å thick Au rectifying contacts were deposited onto this film (for MFS) and front side of *n*-Si (for MS) surface of the wafer through a metal shadow mask by thermal evaporator vacuum system with a pressure of 1×10^{-6} Torr. The thickness of metal layer and deposition rates were both monitored with the help of a digital quartz crystal thickness monitor. This way fabrication of MS and MFS structures were completed and *C–V* and *G*/ω–*V* measurements of the structures were carried out between 10 kHz and 1 MHz at room temperature in the applied bias voltage range of ±5 V using a HP4192A LF impedance analyser with a small a.c. test signal of 40 mV_{rms} from the external pulse generator. *I–V* measurements of the structures were carried out using a Keithley 2400 sourcemeter.

3. Results and discussion

Figures 1 and 2 show *C–V* plots of MS and MFS structures, respectively, along with their *G*/ω–*V* plots as inset figures. Measured data shows that *C* and *G*/ω are dependent on both frequency and applied bias voltage. Judging the frequency dispersion in *C–V* plots, it can be well said that BTO layer's effect in such a way that it diminished structure's dependence on frequency. Moreover, *C–V* plots of both structures exhibit peak behaviour, which is sharper for MFS structure, especially at lower frequencies. This can be due to couple of reasons. First, this may be due to the effects of R_s and N_{ss} which are dominant around the accumulation and depletion regions, respectively, as explained in various studies (Bengi *et al* 2010; Uslu *et al* 2012). As can be seen in figures 1 and 2, the peaks tend to vanish as the frequency is increased; as it is well known, depending on the lifetime of N_{ss} and frequency, N_{ss} can follow a.c. signal and yield excess capacitance at low frequencies (Nicollian and Brews 1982). Also, peak behaviour tends to disappear as the frequency is increased as a result of decreasing effect of excess capacitance in the high frequency range. On the other hand, BTO is a ferroelectric material with fast switching time corresponding to lower switching bias voltage; hence it is expected to have sharp increase in the capacitance values, as a result; sharper peak behaviour is observed

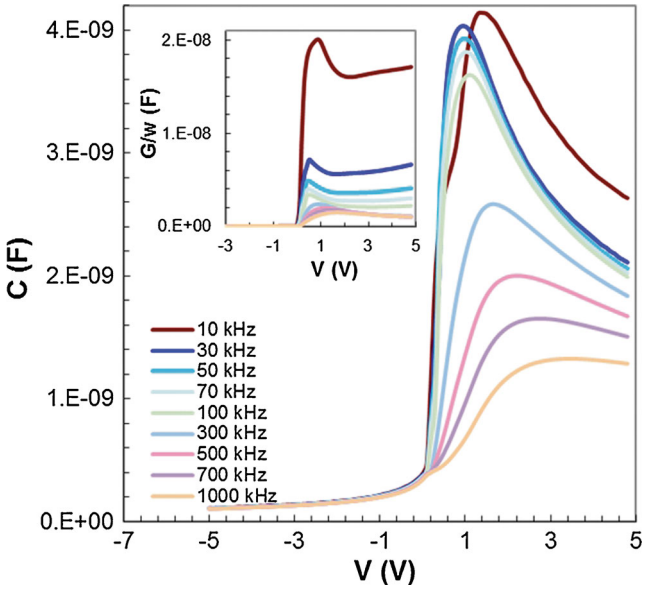

Figure 1. *C–V* plots of MS structure at various frequencies. Inset figure shows *G*/ω–*V* plots.

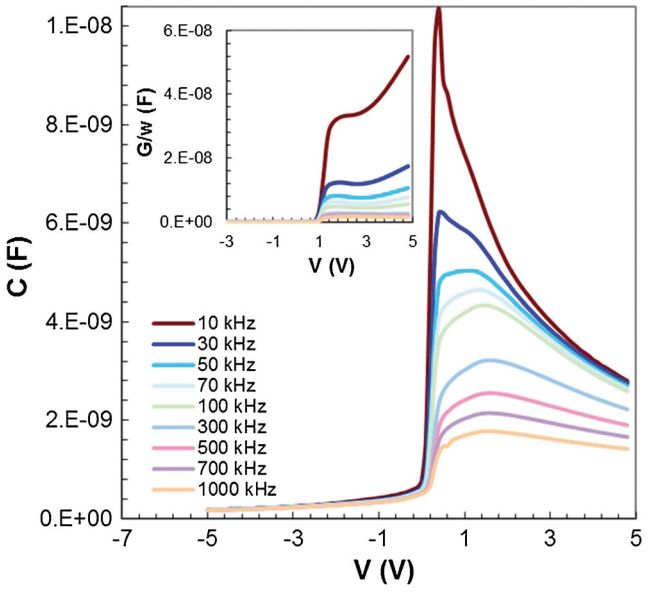

Figure 2. *C–V* plots of MFS structure at various frequencies. Inset figure shows *G*/*ω*–*V* plots.

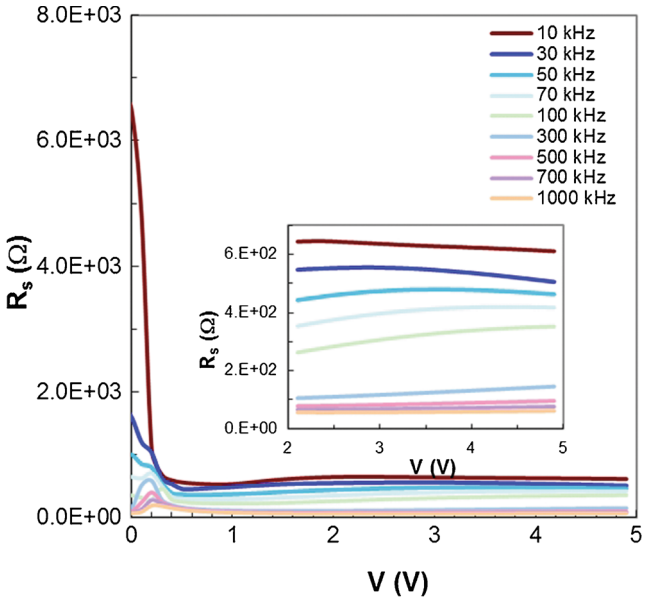

Figure 3. R_i–*V* plots of MS structure at various frequencies. Inset figure shows R_s–*V* plots.

in MFS structure. Furthermore, switching time related with switching voltage of MFS structure is almost preserved as the frequency is increased whereas increasing frequency caused MS structure to have larger switching time and voltage. Thus, frequency dependence of switching time was eliminated through BTO layer. As to *G*/*ω*–*V* plots, BTO layer lead to higher conductance values which implies that BTO layer has diminishing effect on R_s.

When resistivity is considered, R_s appears as an important electrical parameter, because it causes voltage drop of IR_s across the structure, thereby giving rise to small-signal energy loss. There are various methods for extraction of R_s of MS, MFS and similar structures; among them the method proposed by Nicollian and Brews (1982) has been used a lot because of its simplicity. According to this method, R_s of these types of structures are given by the real part of impedance data of accumulation region at sufficiently high frequency level. Considering impedance is the inverse of admittance given by:

$$Y = G + j\omega C, \tag{1}$$

R_s takes the form of:

$$R_s = \frac{G_{ma}}{G_{ma}^2 + (\omega C_{ma})^2}, \tag{2}$$

where C_{ma} and G_{ma} are the measured capacitance and conductance values in accumulation region, and ω is the angular frequency. Equation (2) can also be used to have a general idea about resistivity of a structure. Figures 3 and 4 show R_s–*V* plots of MS and MFS structures along with the inset figures representing the plots of these structures in the accumulation region, respectively. At first glance, R_s–*V* plots reveal that BTO layer led to lower resistance values in

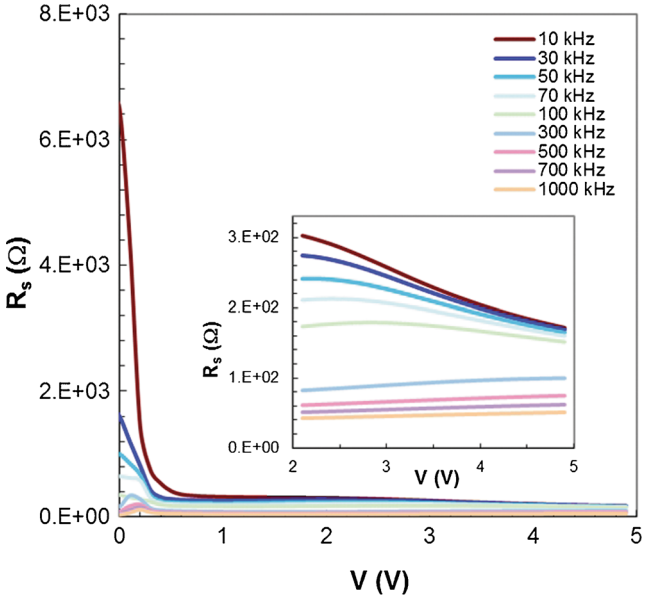

Figure 4. R_i–*V* plots of MFS structure at various frequencies. Inset figure shows R_s–*V* plots.

line with what was predicted through conductance values. Similar behaviour is also observed in the insets of figures 3 and 4 which propose that BTO layer lowered the structure's R_s. As to the frequency dependence, it is seen that R_s increases as frequency is lowered. This can be attributed to N_{ss} of the structures, because N_{ss} takes higher values at lower frequencies which suggests that more charge carriers may be trapped due to higher values of N_{ss}, thus structures become more resistive at low frequencies. In this respect, the fact that

R_s of MS structure, compared to MFS, is more dependent on frequency indicates that N_{ss} of MS structure is larger than that of MFS structure in the accumulation region.

As pointed above, N_{ss} has various effects on MS, MFS and similar structures, and the effect of frequency on N_{ss} depends on the relationship between carrier lifetime of interface trap charges (τ) and $1/\omega$ such that it becomes easier for interface trap charges to follow a.c. signal at lower frequencies ($\tau \ll \omega^{-1}$). Frequency dependence of N_{ss} can be obtained by a method proposed Hill and Coleman (1980). According to this method, frequency dependent N_{ss} values of MS, MFS and similar structures can be obtained by:

$$N_{ss} = \frac{2}{qA} \frac{G_{m,max}/\omega}{\left(\frac{G_{m,max}/\omega}{C_{ox}}\right)^2 + \left(1 - \frac{C_{m,max}}{C_{ox}}\right)^2}, \quad (3)$$

where A is the diode area and $G_{m,max}/\omega$ the measured conductance value at peak point where $C_{m,max}$ corresponds to the capacitance value at the same bias voltage and C_{ox} is the oxide capacitance. As to bias voltage dependent N_{ss} values of these structures, the most commonly used method is the high–low frequency capacitance method proposed by Castange and Vapaille (1971). According to this method, bias voltage dependent N_{ss} values of MS, MFS and similar structures can be obtained by low-frequency capacitance (C_{LF}) and high-frequency capacitance (C_{HF}) data using the following equation:

$$N_{ss} = \frac{1}{qA}\left[\left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1}\right]. \quad (4)$$

Frequency dependent N_{ss} values of MS and MFS structures are given in figure 5 as semi-logarithmic N_{ss}–f plots. As can be seen in figure 5, N_{ss} values of both structures decrease with increasing frequency as expected. At first glance, it seems BTO layer led to higher N_{ss} values; however, this result was obtained for N_{ss} values as a function of frequency. On the other hand, investigation of N_{ss}–V plots can give insight about the response of N_{ss} to applied bias voltage, thus N_{ss} effect can be obtained for different regions. Hence, bias voltage dependent N_{ss}–V plots of these structures are given as inset figure in figure 5. As can be seen, N_{ss} of MFS structure exceeds that of MS structure up to 1 V. However, after this point, N_{ss} values of MFS structure are found smaller in the accumulation region compared to those of MS structure as it was expected through the discussion of R_s. This suggests that, at sufficiently higher bias voltages, BTO layer leads to better interface passivation.

Furthermore, some main electrical parameters of MS, MFS and similar structures can also be obtained using the depletion capacitance data. For these types of structures, N_D can be obtained using the following equation which holds for the depletion region data (Hill and Coleman 1980):

$$C^{-2} = \frac{2(V_{bi} + V)}{q\varepsilon_s A^2 N_D}, \quad (5)$$

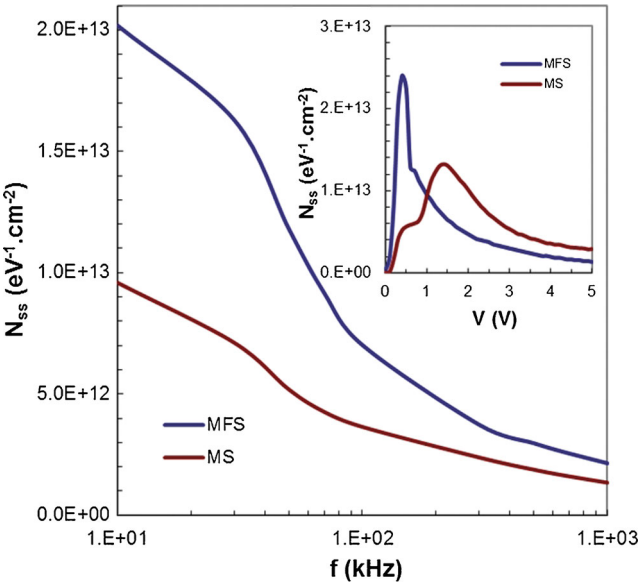

Figure 5. Semilogarithmic N_{ss}–f plots of MS and MFS structures. Inset figure shows N_{ss}–V plots.

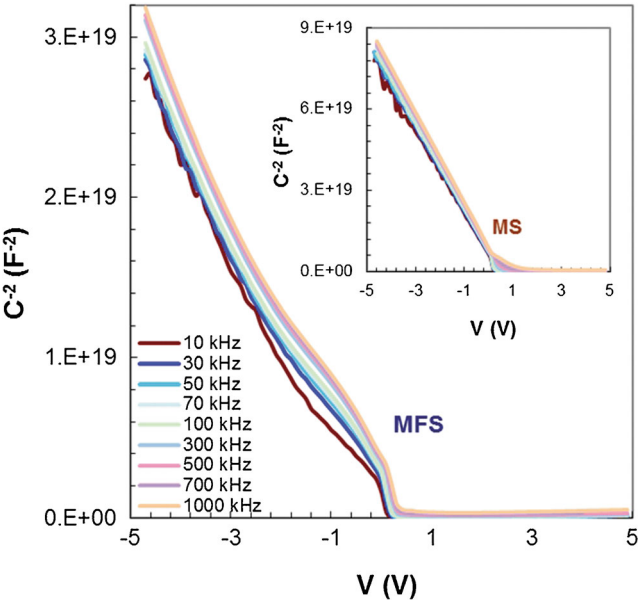

Figure 6. C^{-2}–V plots of MFS structure at various frequencies. Inset figure shows those of MS structure.

where V_{bi} and ε_s are built-in voltage and permittivity of semiconductor, respectively. Therefore, the intercept of C^{-2}–V plot gives V_{bi} and N_D can be easily obtained through the slope value of this plot. Extracting V_{bi} value from C^{-2}–V plot, one can obtain Φ_B value using the following equation:

$$\Phi_B = V_{bi} + \frac{kT}{q} + E_F - \Delta\Phi_B, \quad (6)$$

here, k, T and $\Delta\Phi_B$ are the Boltzmann constant, absolute temperature in Kelvin, Fermi energy and image force barrier

Table 1. Some main electrical parameters obtained from C^{-2}–V plots of MS and MFS structures.

	MS				MFS			
f (kHz)	N_D (cm^{-3})	V_{bi} (V)	E_F (eV)	Φ_B (eV)	N_D (cm^{-3})	V_{bi} (V)	E_F (eV)	Φ_B (eV)
10	3·16E+14	0·455	0·277	0·737	1·39E+15	0·629	0·238	0·860
30	3·09E+14	0·469	0·277	0·748	1·15E+15	0·647	0·243	0·884
50	3·01E+14	0·449	0·278	0·762	1·11E+15	0·694	0·244	0·932
70	3·03E+14	0·492	0·278	0·774	1·08E+15	0·704	0·245	0·943
100	2·98E+14	0·492	0·278	0·775	1·05E+15	0·719	0·246	0·959
300	2·90E+14	0·511	0·279	0·794	1·00E+15	0·778	0·247	1·018
500	2·89E+14	0·521	0·279	0·805	9·82E+14	0·795	0·247	1·036
700	2·87E+14	0·532	0·279	0·816	9·74E+14	0·813	0·248	1·054
1000	2·85E+14	0·540	0·279	0·823	9·64E+14	0·829	0·248	1·070

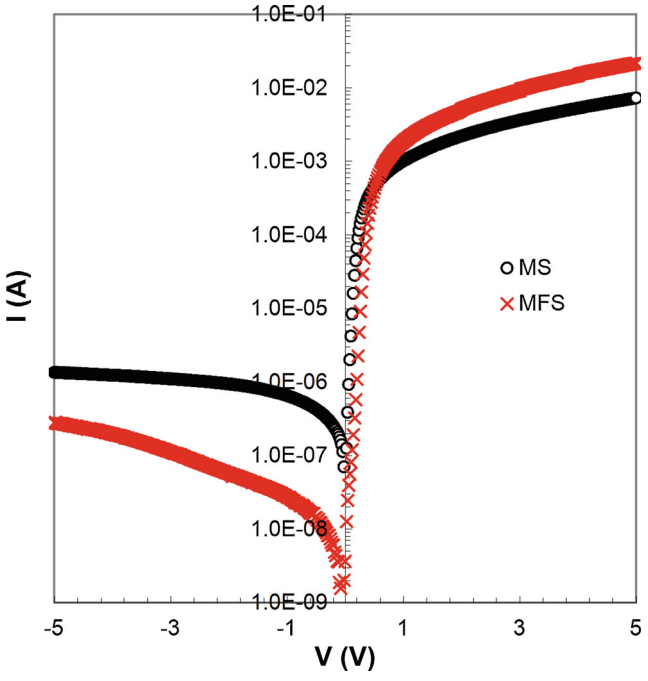

Figure 7. Semilogarithmic I–V plots of MS and MFS structures.

lowering, and the extraction of these parameters was explained in (Yıldırım *et al* 2011). Frequency dependent C^{-2}–V plots of MFS structure are given in figure 6 and those of MS structure are given as inset figure in figure 6. Some main electrical parameters of these structures such as N_D, V_{bi}, E_F and Φ_B are obtained using these plots and given in table 1. As seen in table 1, these parameters' response to frequency is such that V_{bi}, E_F and Φ_B increase with increasing frequency while N_D shows decreasing behaviour. As to the effect of BTO layer on these parameters, increasing behaviour is observed for N_D, V_{bi} and Φ_B after deposition of BTO layer whereas the opposite behaviour holds for E_F.

Figure 7 shows the semi-logarithmic I–V plots of MS and MFS structures at room temperature. As can be seen in the figure, MFS structure has a larger rectifying ratio thanks to higher current values in the forward bias region and lower leakage current values in the reverse bias region. In these kinds of structures, current passing through the structure is expressed as (Gökçen and Yıldırım 2012)

Table 2. Some main electrical parameters obtained from I–V plots of MS and MFS structures.

	I_o (A)	n	Φ_{Bo} (eV)
MS	1·1E−7	1·08	0·71
MFS	2·3E−9	1·23	0·80

$$I = \underbrace{AA^*T^2 \exp\left(-\frac{q\Phi_{Bo}}{kT}\right)}_{I_o}\left[\exp\left(\frac{q(V - IR_s)}{nkT}\right) - 1\right], \tag{7}$$

where A^* is the effective Richardson constant (120 A/cm^2·K^2 for n-Si), I_o the reverse saturation current, n the ideality factor and Φ_{Bo} the apparent barrier height at zero-bias. I_o, n and Φ_{Bo} are calculated and given in table 2 using (7) and the linear section in I–V plots of the structures approximately between 0 and 0·5 V. The extraction of these parameters are explained in Nanda Kumar Reddy and Rajagopal Reddy (2012). As can be seen, the interfacial BTO layer led to lower I_o value whereas, it increased n and Φ_{Bo} values of the structure. n values of the MFS structure is larger than unity, however this value is acceptable since it is close to 1. When we consider the barrier height values; it is seen that Φ_B values obtained by C^{-2}–V plots are larger than Φ_{Bo} values obtained by I–V plots. This is due to the fact that Φ_B, the barrier height from rectifier metal contact to semiconductor, is calculated using reverse-bias and Φ_{Bo}, the barrier height from semiconductor to rectifier metal contact, is calculated using forward-bias data, therefore Φ_B is larger than Φ_{Bo} by approximately Fermi energy. In this sense, it can be said that the barrier height values obtained from I–V and C^{-2}–V plots are in agreement with each other.

4. Conclusions

C–V and *G*/*ω*–*V* characteristics of the fabricated MS and MFS structures measured between 10 kHz and 1 MHz at room temperature were investigated for the purpose of studying the effects of ferroelectric BTO layer on the main electrical parameters of these structures. BTO layer caused sharp peak behaviour in *C–V* plots which was attributed mainly to peculiar switching ability of BTO besides the effects of R_s and N_{ss}. Results also showed that BTO layer caused increment in conductance values and this indicated that BTO could have diminishing effect on resistivity. This was verified once R_s–*V* plots were obtained. These plots showed that R_s of MFS structure is less dependent to frequency compared to MS structure, this result suggested that N_{ss} of MFS structure should be smaller in the accumulation region. This was confirmed by calculating bias voltage dependent N_{ss} using high–low frequency method and attributed to surface passivation in accumulation region through BTO layer. Furthermore, it was found that BTO layer increased N_D, V_{bi} and Φ_B while it decreased E_F. *I–V* characteristics also showed BTO caused improvements in the structure's electrical characteristics. The values of electrical parameters, such as barrier height, obtained from *I–V* and C^{-2}–*V* characteristics are in consistency with each other considering the barrier from metal to semiconductor is supposed to be larger than the one from semiconductor to metal.

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