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A new hysteresis band current control technique for a shunt active filter

Murat KALE[1,*], **Engin ÖZDEMİR**[2]

[1]Department of Electrical and Electronics Engineering, Faculty of Technology, Düzce University, Düzce University, Turkey

[2]Department of Energy Systems Engineering, Faculty of Technology, Kocaeli University, Kocaeli, Turkey

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Abstract: This paper proposes a hysteresis band (HB) current control technique to reduce the power losses in a shunt active filter. During a switching period in the zero-crossing region, the inverter output current flows through a transistor. By changing the direction, it flows through the free-wheeling diode of the same switch in an inverter leg, or vice versa. The shunt active filter current typically has 6 zero-crossing regions during a fundamental frequency cycle. This paper presents a HB current control technique where there is not any switching in these 6 zero-crossing regions per period, which results in reducing the power losses. The experimental results clearly show that the power losses of the shunt active filter are reduced by using the proposed technique.

Key words: Harmonics, shunt active filter, hysteresis band current control, power losses

1. Introduction

The rapid increase of power electronic devices (i.e. rectifiers, inverters, and AC electric arc furnaces) in industrial applications has caused important power quality problems, such as harmonic currents and reactive power in the electric power system. These devices, which are also called nonlinear loads, draw nonsinusoidal currents and reactive power from the electric power system. In order to solve these problems, shunt active filters have been reported [1–4] and considered as a possible solution for the harmonic current compensation.

The shunt active filter operates as a current controlled voltage source inverter connected in parallel with the nonlinear load. To obtain the current references, which need to be produced by the voltage source inverter for the harmonic current compensation, the instantaneous reactive power theory proposed by Akagi [1] is used in this study. The output current of the shunt active filter is controlled by using different current control techniques. The most commonly used current control techniques in the shunt active filters was presented in [5]. For the application of the active filter, the hysteresis band (HB) current control technique is the most preferred solution because of advantages such as easy implementation and a very fast dynamic response [5–13].

The main reason for choosing a current control technique is high efficiency. In order to improve the efficiency of the voltage source inverter, the chosen current control technique should reduce the power losses of the voltage source inverter by lowering the switching frequency [14]. Some recent studies that reduced the power losses of the voltage source inverter in the HB current control technique were reported in [15–23]. In [15–17], hysteresis comparators with a lookup table were used to decrease the inverter switching frequency selecting zero voltage vectors. In [18,19], the hysteresis current control methods with minimal switching using phase voltage

*Correspondence: muratkale@duzce.edu.tr

segmentation for a 3-phase 3-wire system and extending for a 3-phase 4-wire system were presented, respectively. In [20,21], a double band hysteresis current controller was proposed for the single-phase full-bridge pulse-width modulation (PWM) inverter to utilize the zero voltage level, and in [22], a hysteresis current controller that combined the advantages of both the conventional double band hysteresis current controller and symmetrical unipolar PWM was presented. In [23], a discontinuous pulse width modulation technique to reduce switching losses was presented.

In the conventional HB current control technique, maximum switching frequency occurs near the zero-crossing region [7–9]. Additionally, in the zero-crossing region shown in Figure 1, the inverter output current flows through a transistor, and then, by changing the direction, it flows through a free-wheeling diode of the same transistor during a switching period, or vice versa. This study presents a detailed analysis related to these zero-crossing regions and accordingly proposes a HB current control technique to reduce the power losses of the shunt active filter by avoiding the switching in the zero-crossing regions. In the proposed technique, two switches of an inverter leg are controlled independently, avoiding the two switches of the same leg that are also in the "on" state. According to the proposed technique, the two switches of an inverter leg are in the "off" state in the zero-crossing region. In the currents produced by the shunt active filter, there are 6 zero-crossing regions during a fundamental frequency cycle passing without any switching in the proposed technique. Experimental studies are carried out and the effect of the proposed method on reducing the power losses of the shunt active filter is verified. The remainder of the paper is organized as follows: in the second section, the 3-phase 4-wire shunt active filter with split capacitor is described. The analysis of the conventional HB current control technique in the zero-crossing region is introduced in the third section. The proposed HB current control technique for reducing power losses is given in the fourth section. The fifth section consists of the experimental results obtained from different operating conditions and comparisons of the conventional and proposed methods. In the sixth section, conclusions are presented.

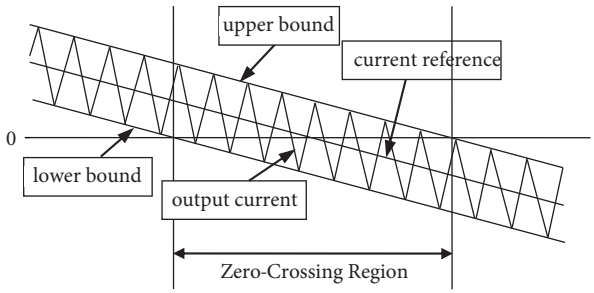

Figure 1. Zero-crossing region.

2. Three-phase 4-wire shunt active filter with split capacitor

The configuration of a 3-phase 4-wire shunt active filter with split capacitor is shown in Figure 2. The power circuit of the shunt active filter contains a 3-phase inverter and 2 DC capacitors connected to the DC bus. The midpoint of these capacitors is connected to the neutral return path for compensating the neutral current. In this topology, two capacitor voltages are sensed to obtain the DC bus voltage ($v_{dc}(t) = v_{dc1}(t) + v_{dc2}(t)$) and the differential voltage ($v_{dc1} - v_{dc2}$) [13,24]. To maintain the desired DC bus voltage level and to balance the voltage level of these capacitors, 2 control loops are needed, as shown in Figure 3. The first control loop, which is used for compensating the active filter losses and maintaining the desired DC bus voltage level, is in the d-axis. The second one, which is used for maintaining the DC voltage balance, is in the 0-axis.

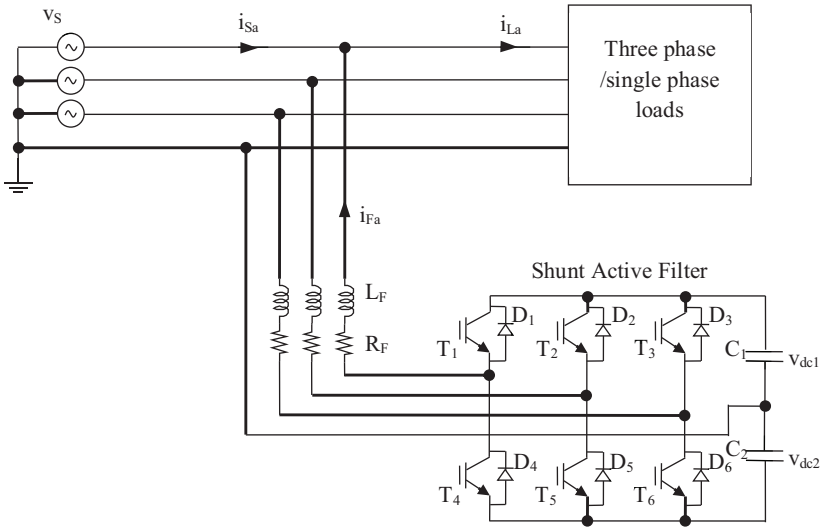

Figure 2. Configuration of the shunt active filter.

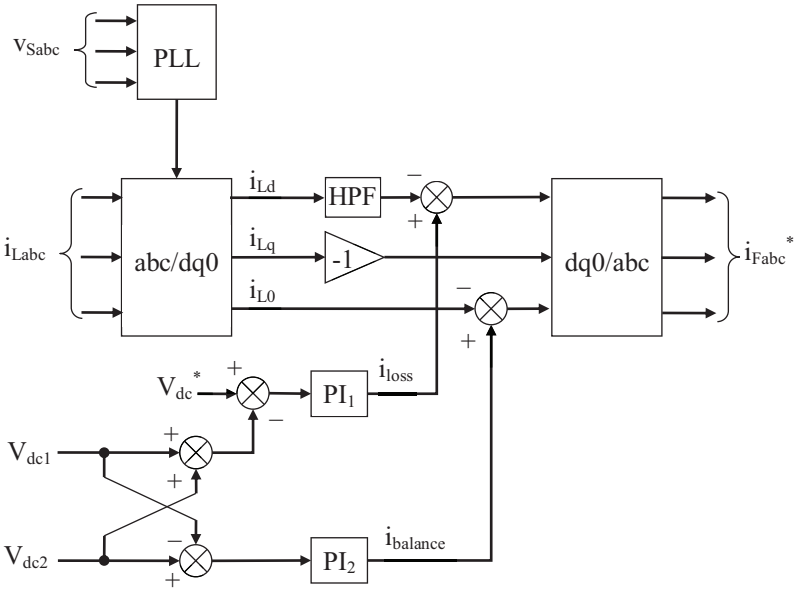

Figure 3. The control block diagram of the shunt active filter.

In order to compensate load harmonic currents and to ensure that the source currents are in phase with the source voltages, the 3-phase supply voltages and the 3-phase load currents are sensed. For reference frame transformation, the transformation matrix that was used is given in Eq. (1).

$$T_{dq0}^{abc} = \frac{2}{3}\begin{bmatrix} \sin(\omega t) & \sin(\omega t - 2\pi/3) & \sin(\omega t + 2\pi/3) \\ \cos(\omega t) & \cos(\omega t - 2\pi/3) & \cos(\omega t + 2\pi/3) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{1}$$

The load currents are transformed into a synchronous reference frame as follows:

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \\ i_{L0} \end{bmatrix} = T_{dq0}^{abc} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix}. \tag{2}$$

The currents in the synchronous reference frame have DC and AC signals. Among these signals, i_{Lq}, i_{L0}, and the AC part of i_{Ld} are unwanted signals because they are parts of the load currents that respectively represent reactive currents, unbalanced currents, and harmonic currents. In order to compensate for these unwanted signals, to regulate the DC bus voltage, and to balance the DC level of the capacitors, current references are calculated in Eq. (3). The oscillating part of the d-axis current used in Eq. (3) can be obtained by using a high-pass filter.

$$\begin{bmatrix} i_{Fa}^{*} \\ i_{Fb}^{*} \\ i_{Fc}^{*} \end{bmatrix} = T_{abc}^{dq0} \begin{bmatrix} -\tilde{i}_{Ld} + i_{loss} \\ -i_{Lq} \\ -i_{L0} + i_{balance} \end{bmatrix}, \tag{3}$$

where the reference frame transformation matrix is given as follows:

$$T_{abc}^{dq0} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) & 1 \\ \cos(\omega t - 2\pi/3) & \sin(\omega t - 2\pi/3) & 1 \\ \cos(\omega t + 2\pi/3) & \sin(\omega t + 2\pi/3) & 1 \end{bmatrix}. \tag{4}$$

i_{loss} is the active current required to maintain the DC bus voltage at the desired level, ($V_{dc}*$), and to compensate the losses associated with the power circuit of the shunt active filter [1,12,24,25]. The i_{loss} signal is calculated as:

$$\begin{aligned} e_1(t) &= V_{dc}^{*} - (v_{dc1}(t) + v_{dc2}(t)) \\ i_{loss} &= k_{p1} e_1(t) + k_{i1} \int_0^t e_1(\tau) d\tau \end{aligned}, \tag{5}$$

where $e_1(t)$ is the error signal between the reference value of the DC bus voltage ($V_{dc}*$) and the instantaneous DC bus voltage ($v_{dc}(t) = v_{dc1}(t) + v_{dc2}(t)$), and k_{p1} and k_{i1} constants are proportional and integral gain of the PI_1 controller.

$i_{balance}$ is used for balance between v_{dc1} and v_{dc2} capacitor voltages. The $i_{balance}$ signal is calculated as:

$$\begin{aligned} e_2(t) &= (v_{dc1}(t) - v_{dc2}(t)) \\ i_{balance} &= k_{p2} e_2(t) + k_{i2} \int_0^t e_2(\tau) d\tau \end{aligned}, \tag{6}$$

where $e_2(t)$ is the error signal between v_{dc1} and v_{dc2} voltages, and k_{p2} and k_{i2} constants are proportional and integral gain of the PI_2 controller.

3. Analysis of the conventional HB current control technique in the zero crossing region

In the HB current control technique, the switching signal is produced directly when the current error exceeds the HB [6]. The block scheme of the conventional HB current control technique and an inverter leg of the

3-phase 4-wire shunt active filter is shown in Figure 4. In this figure, i^*_{Fa} is the current reference and i_{Fa} and v_{Fa} are the inverter output current and voltage, i_{T1} and i_{D1} are T_1 transistor and D_1 diode currents, and i_{T2} and i_{D2} are T_2 transistor and D_2 diode currents, respectively. The current reference (i^*_{Fa}) is compared with the sensed output current (i_{Fa}), and by using the resulting error, the hysteresis band controller (HBC) derives the switching signals.

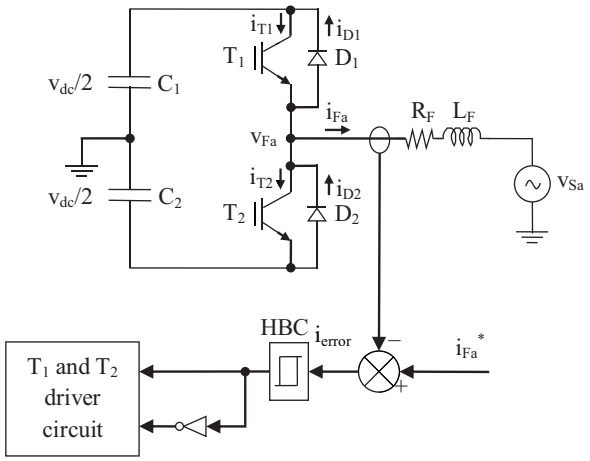

Figure 4. The basic scheme of the conventional HB current control technique.

In the conventional HB current control technique, the switching signals are sent to the T_1 and T_2 transistors by the HBC. As shown in Figure 4, the output of the HBC is directly connected to the T_1 transistor, and by taking the reverse of it, it is connected to the T_2 transistor. Therefore, both of the switches at the same leg cannot be in the "on" state or "off" state. In this technique, the output current is kept between the lower bound and the upper bound of the HB. The algorithm of the conventional HB is given as follows:

$$\begin{array}{l} \text{if } i_{Fa} \leq (i^*_{Fa} - HB) \text{ then } T_1 = \text{`}on\text{'} \text{ and, } T_2 = \text{ `off'} \\ \text{if } i_{Fa} \geq (i^*_{Fa} + HB) \text{ then } T_1 = \text{ `off' and } T_2 = \text{ `on'} \end{array} .$$

In the conventional HB current control technique, the switching period consists of 4 different operation modes in the zero-crossing region. These modes and the key waveforms concerning the operation modes are given in Figure 5. The equivalent circuits of each of the operation modes are shown in Figure 6. The operation modes in the zero-crossing region are explained below.

Mode 1 $[t_1 - t_2]$ (Figure 6a): This mode starts when the output current (i_{Fa}) reaches the upper bound of the HB. At the beginning of this stage, the HBC sends the turn-off signal to the T_1 transistor and the turn-on signal to the T_2 transistor. In this mode, the T_1 and T_2 transistors and the D_1 diode are in the "off" state and the D_2 diode is in the "on" state. During this mode, the output current flows through the D_2 diode ($i_{D2} = i_{Fa}$). This stage ends at t_2 when the output current (i_{Fa}) reaches zero. At the end of this stage, the D_2 diode is in the "off" state. In this mode, v_{Fa} is $-V_{dc}/2$.

Mode 2 $[t_2 - t_3]$ (Figure 6b): Since the output current does not reach the lower bound of the HB, the turn-on signal that was applied to the T_2 transistor at the beginning of Mode 1 still remains unchanged during Mode 2. In this mode, the D_1 and D_2 diodes and the T_1 transistor are in the "off" state, and the T_2 transistor is in the "on" state. During this mode, the output current flows through the T_2 transistor ($i_{T2} = i_{Fa}$). This stage ends at t_3 when the output current (i_{Fa}) reaches the lower bound of the HB. At t_3, the HBC sends the

turn-off signal to the T_2 transistor. At the end of this stage, the T_2 transistor is in the "off" state. In this mode, v_{Fa} is $-V_{dc}/2$.

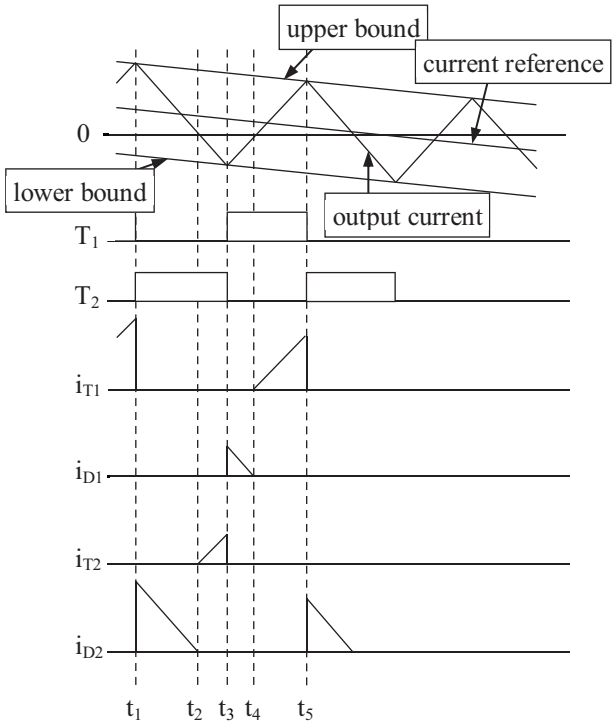

Figure 5. Operating waveforms in the zero-crossing region in the conventional current control technique.

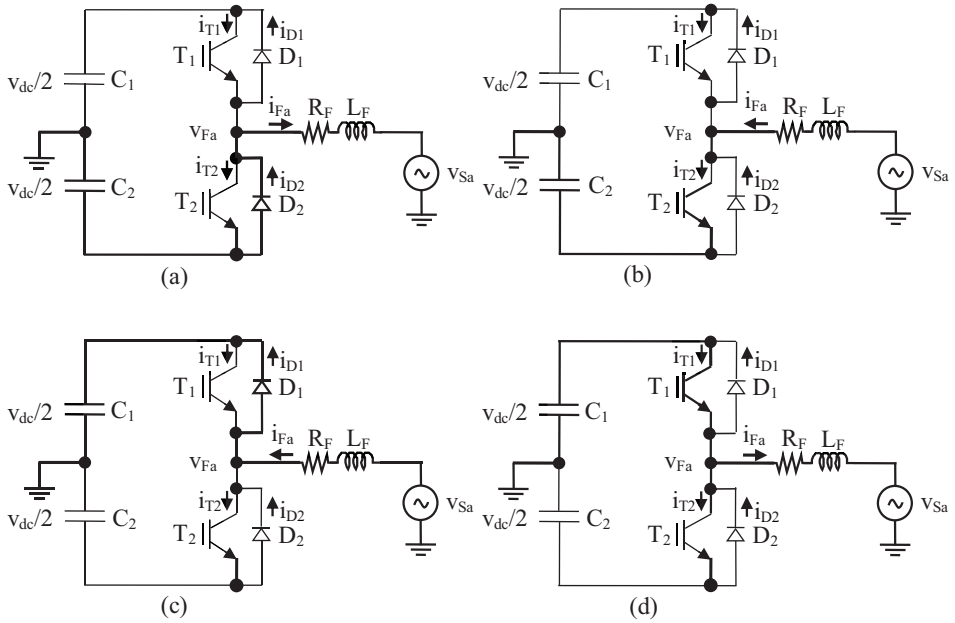

Figure 6. Equivalent circuits of the operation modes in the conventional current control technique: a) Mode 1, b) Mode 2, c) Mode 3, d) Mode 4.

Mode 3 $[t_3 - t_4]$ (Figure 6c): At the beginning of this stage, the HBC sends the turn-on signal to the T_1 transistor. In this mode, the T_1 and T_2 transistors and the D_2 diode are in the "off" state, and the D_1 diode is in the "on" state. During this mode, the output current flows through the D_1 diode ($i_{D1} = i_{Fa}$). This stage ends at t_4 when the output current (i_{Fa}) reaches zero. At the end of this stage, the D_1 diode is in the "off" state. In this mode, v_{Fa} is $V_{dc}/2$.

Mode 4 $[t_4 - t_5]$ (Figure 6d): The turn-on signal that was applied to the T_1 transistor at the beginning of mode 3 remains unchanged during mode 4, and because of that, the output current does not reach the upper bound of the HB. In this mode, the T_2 transistor and the D_1 and D_2 diodes are in the "off" state, and the T_1 transistor is in the "on" state. During this mode, the output current flows through the T_1 transistor ($i_{T1} = i_{Fa}$). This stage ends at t_5 when the output current (i_{Fa}) reaches the upper bound of the HB. At t_5, the HBC sends the turn-off signal to the T_1 transistor. At the end of this stage, the T_1 transistor is in the "off" state. In this mode, v_{Fa} is $V_{dc}/2$.

4. The proposed HB current control technique

The main objective of the proposed technique is passing without any switching in the zero-crossing regions to reduce the power losses. In this study, it is achieved by using two HB controllers, where one is connected to the upper switch and the other is connected to the lower switch of an inverter leg. The algorithms of the upper and the lower HBC connected to the T_1 and T_2 transistors are given as follows.

For T_1:

$$\begin{array}{l} \text{if } i_{Fa} \leq (i^*_{Fa} - HB) \text{ then } T_1 = \text{ 'on'} \\ \text{if } i_{Fa} \geq i^*_{Fa} \text{ then } T_1 = \text{ 'off'} \end{array} .$$

For T_2:

$$\begin{array}{l} \text{if } i_{Fa} \geq (i^*_{Fa} + HB) \text{ then } T_2 = \text{ 'on'} \\ \text{if } i_{Fa} \leq i^*_{Fa} \text{ then } T_2 = \text{ 'off'} \end{array} .$$

Due to the algorithms of the HBCs connected to both of the switches of an inverter leg, the output current is maintained between the lower bound of the HB and the current reference when the current reference is positive, and it is between the current reference and the upper bound of the HB when the current reference is negative. The principle block diagram of the proposed HB current control technique is given in Figure 7.

In the conventional HB current control technique, the HBC applies the turn-on signal to the transistor even though the output current does not flow through the transistor as mentioned for Mode 1 and Mode 3 in Section 2 and as clearly shown in Figure 7. In the proposed HB current control technique, due to the algorithm, the turn-on signal is not applied to the gate of the transistor while the output current is flowing through the free-wheeling diode of the transistor.

According to the proposed HB current control technique, two transistors of the same leg cannot be in the "on" state, but they can be in the "off" state in the zero-crossing region. The switching period consists of 3 different operation modes in the zero-crossing region. These modes and the key waveforms concerning the operation modes are given in Figure 8, and the equivalent circuits of each operation mode are shown in Figure 9. The operation modes in the zero-crossing region are explained as follows.

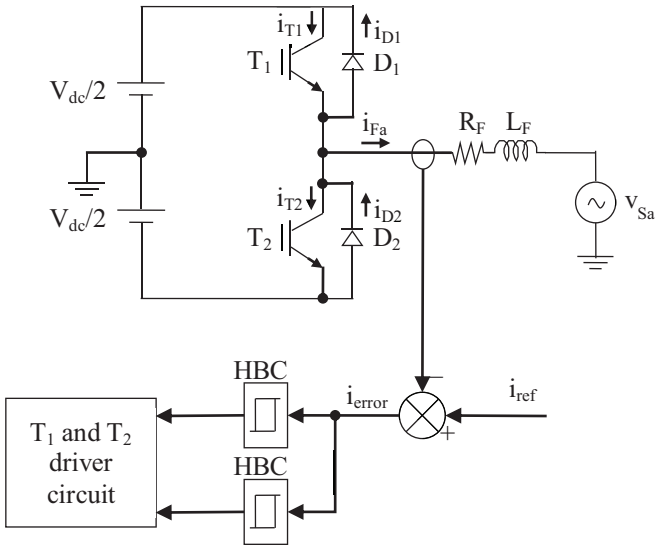

Figure 7. The proposed HB current control technique.

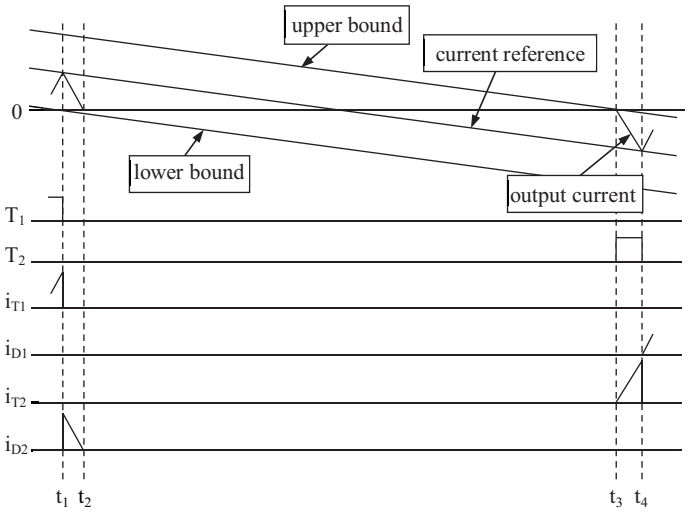

Figure 8. Operating waveforms in the zero-crossing region in the proposed current control technique.

Mode 1 $[t_1 - t_2]$ (Figure 9a): This mode starts when the output current (i_{Fa}) reaches the upper bound of the HB. At the beginning of this stage, the HBC sends the turn-off signal to the T_1 transistor. Contrary to the conventional HB current controller technique, as mentioned in Section 2, while the current is flowing through the D_2 diode, the turn-on signal is not applied to the T_2 transistor in the proposed HB current control controller technique. In this mode, the T_1 and T_2 transistors and the D_1 diode are in the "off" state and the D_2 diode is in the "on" state. During this mode, the output current flows through the D_2 diode ($i_{D2} = i_{Fa}$). This stage ends at t_2 when the output current (i_{Fa}) reaches zero. At the end of this stage, the D_2 diode is in the "off" state. In this mode, v_{Fa} is $-V_{dc}/2$.

Mode 2 $[t_2 - t_3]$ (Figure 9b): This mode starts when the output current reaches zero. Unlike the conventional HB current control technique, the output current does not reach the lower bound of the HB, since the turn-on signal is not applied to the T_2 transistor. In this mode, the T_1 and T_2 transistors and the D_1 and D_2 diodes are in the "off" state. During this mode, $i_{T1} = i_{T2} = i_{D1} = i_{D2} = i_{Fa} = 0$ and $v_{Fa} = 0$. This

stage ends at the end of the zero-crossing region at t_3.

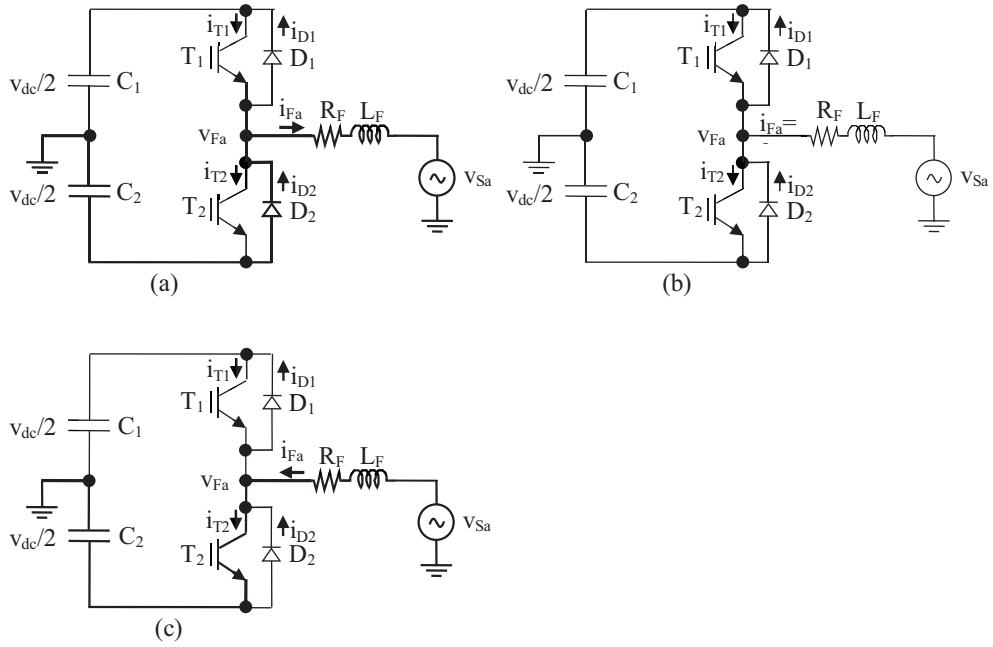

Figure 9. Equivalent circuits of the operation modes in the proposed current control technique: a) Mode 1, b) Mode 2, c) Mode 3.

Mode 3 $[t_3 - t_4]$ (Figure 9c): This mode starts when the upper bound of the HB reaches zero. The proposed HBC sends the turn-on signal to the T_2 transistor. In this mode, the T_1 transistor and the D_1 and D_2 diodes are in the "off" state and the T_2 transistor is in the "on" state. During this mode, the output current flows through the T_2 transistor ($i_{T2} = i_{Fa}$). This stage ends at t_4 when the output current (i_{Fa}) reaches the current reference. At t_4, the HBC sends the turn-off signal to the T_2 transistor. At the end of this stage, the T_2 transistor is in the "off" state. In this mode, v_{Fa} is $-V_{dc}/2$.

5. Experimental results

In order to verify the validity of the proposed current control technique, a laboratory prototype was assembled, and both the conventional technique and the proposed technique were tested under the same operating conditions. The system parameters of the nonlinear load and the shunt active filter are given in the Table. In the laboratory setup, line to neutral voltage was 55 V with 50 Hz. The nonlinear load was a 3-phase diode rectifier with a resistive-inductive load. The shunt active filter consisted of a 3-phase voltage source inverter with a split capacitor. The inverter had 6 IRG4PH50KD IGBTs driven by SKYPER 32 PRO, which has 3.3 μs of hardware dead time. For measuring the source voltages, load currents, filter currents, and DC bus voltages, Hall-effect voltage (LV-25P) and current (LA55P) sensors were used. To control the system, a TMS320F28335 Experimenter Kit was used. Sampling frequency was selected as 50 kHz.

The tests were carried out at different HB widths in order to compare the proposed technique with the conventional technique. For 0.5-A HB width, the experimental results obtained from the conventional technique are presented in Figure 10. The total harmonic distortion (THD) of the load current shown in Figure 10a is 24.55%. The filter current is shown in Figure 10b. The THD of the source current shown in Figure 10c is 4.47%.

For 0.5-A HB width, the experimental results obtained from the proposed technique are presented in Figure 11. The THD of the load current shown in Figure 11a is 24.32%. The filter current is shown in Figure 11b. The THD of the source current shown in Figure 11c is 4.77%. Due to the zero-crossing regions, the power losses of the shunt active filter are reduced compared to the conventional technique.

Table. System parameters.

Parameters	Symbols	Value
Source		
Voltage (line-neutral)	v_{Sabc}	55 V_{rms}
Frequency	f	50 Hz
Three-phase load		
AC line inductance and resistor	L_{AC}, R_{AC}	1 mH, 0.2 Ω
DC inductance and resistor	L_{DC}, R_{DC}	40 mH, 13 Ω
Shunt active power filter		
DC link voltage	V_{DC}	180 V
DC link capacitor	C_{DC}	1100 μF
AC line inductance and resistor	L_F, R_F	3 mH, 0.3 Ω

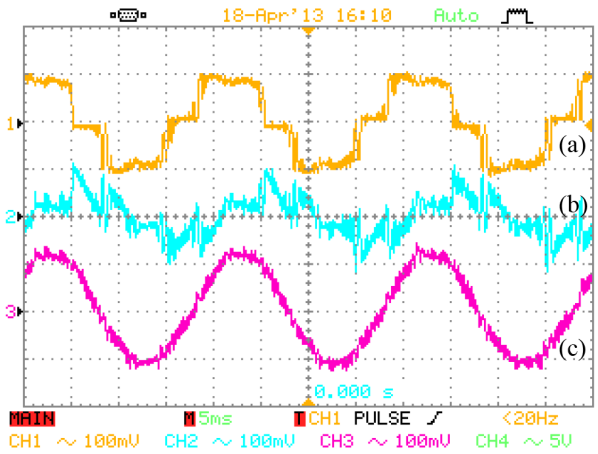

Figure 10. Experimental results of the conventional technique: a) the load current, b) the filter current, c) the source currents.

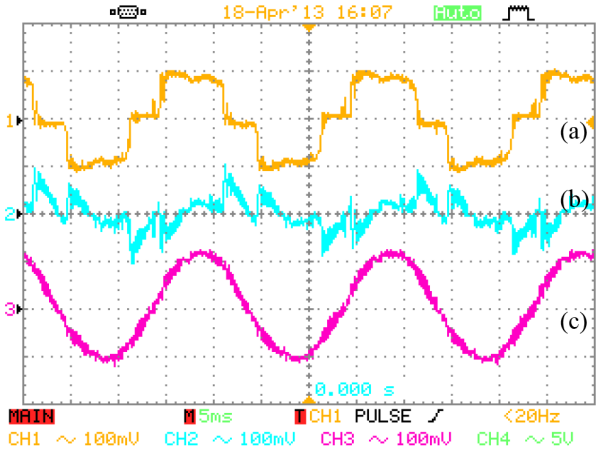

Figure 11. Experimental results of the proposed technique: a) the load current, b) the filter current, c) the source currents.

The THD value of the source current and the power losses with the various HB widths for both the conventional technique and the proposed technique are shown in Figure 12. The power losses are obtained by subtracting the 3-phase nonlinear load power from the 3-phase power drawn from the electric power system. To measure the power, a HIOKI 3196 power quality analyzer was used. Figures 12a and 12b show the THD value of the source current and power losses. Using Figures 12c and 12d, the power losses and the efficiency of the conventional technique can be easily compared with the proposed technique at the same THD value of the source current. In Figure 12, it is clearly shown that the proposed technique is more efficient than the conventional technique.

6. Conclusion

In this study, a HB current control technique is proposed for the shunt active filter. The proposed current controller reduces the power losses because there is not any switching in the zero-crossing regions. The current of the shunt active filter current typically has 6 zero-crossing regions. Using the proposed technique, the efficiency of the shunt active filter is improved. The proposed technique and the conventional technique are compared at different HB widths. The experimental results show that the proposed technique causes less power loss compared with the conventional technique at the same source current THD value. The experimental results validate the performance and the feasibility of the proposed method.

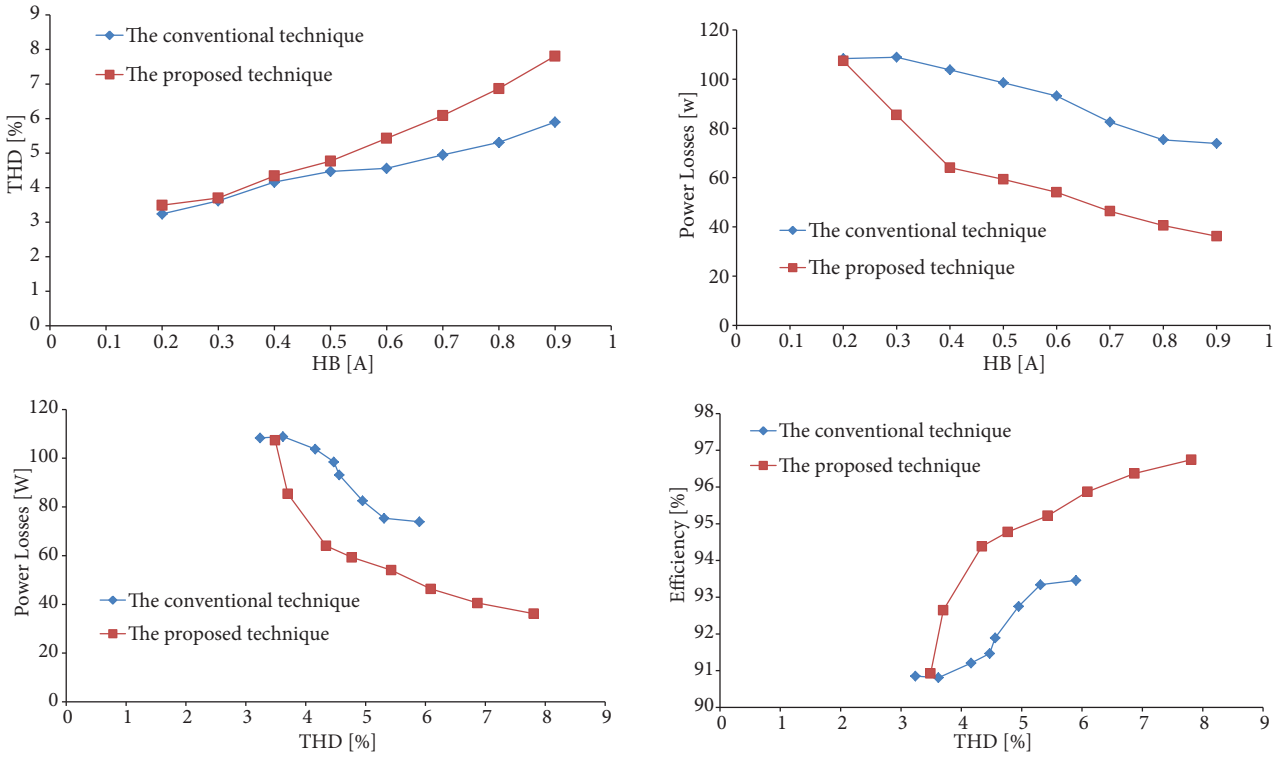

Figure 12. a) HB width-THD, b) HB width-power losses, c) THD-power losses, d) THD-efficiency of the conventional technique and the proposed technique.

References

[1] Akagi H, Kanazawa Y, Nabae A. Instantaneous reactive power compensators comprising switching devices without energy storage components. IEEE T Ind Appl 1984; IA-20: 625–630.

[2] Akagi H. New trends in active filters for power conditioning. IEEE T Ind Appl 1996; 32: 1312–1322.

[3] Singh B, Al-Haddad K, Chandra A. A review of active filters for power quality improvement. IEEE T Ind Electron 1999; 46: 960–971.

[4] Watanabe HE, Akagi H, Aredes M. Instantaneous p-q power theory for compensating nonsinusoidal systems. In: International School on Nonsinusoidal Currents and Compensation; 10–13 June 2008; Lagow, Poland. New York, NY, USA: IEEE, 2008. pp. 1–10.

[5] Buso S, Malesani L, Mattavelli P. Comparison of current control techniques for active filter applications. IEEE T Ind Electron 1998; 45: 722–729.

[6] Kazmierkowski MP, Malesani L. Current control techniques for three-phase voltage source PWM converters: a survey. IEEE T Ind Electron 1998; 45: 691–703.

[7] Holtz J. Pulsewidth modulation: a survey. IEEE T Ind Electron 1992; 39: 410–420.

[8] Rahman MA, Radwan TS, Osheiba AM, Lashine AE. Analysis of current controllers for voltage-source inverter. IEEE T Ind Electron 1997; 44: 477–485.

[9] Rahman KM, Khan MR, Choudhury MA, Rahman MA. Variable-band hysteresis current controllers for PWM voltage-source inverters. IEEE T Power Electron 1997; 12: 964–970.

[10] Buso S, Fasolo S, Malesani L, Mattavelli P. A dead-beat adaptive hysteresis current control. IEEE T Ind Appl 2000; 36: 1174–1180.

[11] Kale M, Ozdemir E. An adaptive hysteresis band current controller for shunt active power filter. Electric Power Syst Res 2005; 73: 113–119.

[12] Ucar M, Ozdemir E. Control of a 3-phase 4-leg active power filter under non-ideal mains voltage condition. Electric Power Syst Res 2008; 78: 58–73.

[13] Uçar M, Özdemir Ş, Özdemir E. A unified series-parallel active filter system for nonperiodic disturbances. Turk J Electr Eng Co 2011; 19: 575–596.

[14] Zeng J, Ni Y, Diao Q, Yuan B, Chen S, Zhang B. Current controller for active power filter based on optimal voltage space vector. IEE P-Gener Transm D 2001; 148: 111–116.

[15] Kaimierkowski MP, Dzieniakowski MA, Sulkowski W. Novel space vector based current controllers for PWM-inverters. IEEE T Power Electron 1991; 6: 158–166.

[16] Pan CT, Chang TY. An improved hysteresis current controller for reducing switching frequency. IEEE T Power Electron 1994; 9: 97–104.

[17] Kwon BH, Kim TW, Youm JH. A novel SVM-based hysteresis current controller. IEEE T Power Electron 1998; 13: 297–307.

[18] Kumar MN, Vasudevan K. Bi-directional real and reactive power control using constant frequency hysteresis control with reduced losses. Electric Power Syst Res 2005; 76: 127–135.

[19] Lohia P, Mishra MK, Karthikeyan K, Vasudevan K. A minimally switched control algorithm for three-phase four-leg VSI topology to compensate unbalanced and nonlinear load. IEEE T Power Electron 2008; 23: 1935–1944.

[20] Kato T, Miyao K. Modified hysteresis control with minor loops for single-phase full-bridge inverters. In: Industry Applications Society Annual Meeting; 2–7 October 1988; Pittsburgh, PA, USA. New York, NY, USA: IEEE. pp. 689–693.

[21] Lo YK, Chiu HJ, Ou SY. Dual hysteresis loops for a high performance four-switch boost rectifiers. IEEE T Ind Electron 2000; 47: 1174–1176.

[22] Dahono PA. New hysteresis current controller for single-phase full-bridge inverters. IET Power Electron 2009; 2: 585–594.

[23] Asiminoaei L, Rodríguez P, Blaabjerg F. Application of discontinuous PWM modulation in active power filters. IEEE T Power Electron 2008; 23: 1692–1706.

[24] Khadkikar V, Chandra A, Singh B. Digital signal processor implementation and performance evaluation of split capacitor, four-leg and three H-bridge-based three-phase four-wire shunt active filters. IET Power Electron 2011; 4: 463–470.

[25] Ucar M, Ozdemir S, Ozdemir E. A four-leg unified series-parallel active filter system for periodic and non-periodic disturbance compensation. Electric Power Syst Res 2011; 81: 1132–1143.